1. BF7612DMXX-SJLX MCU General Description

1.1. Features

- **Core: high-speed 8051**
  - Operating frequency: 12MHz, 6MHz, 4MHz, 1MHz
  - Clock error: ±1% @-20 ℃~65 ℃, 5V
    ±3% @-40 ℃~105 ℃, 5V
- **Memory (SMTP)**
  - CODE: 16K Bytes
  - DATA: 1K Bytes
  - SRAM: 256 Bytes(data)+512 Bytes(xdata)
  - Support BOOT function area, 1/2/3/4K selected
- **Clock source, reset and power management**
  - Internal low-speed clock LIRC: 32kHz,
    Clock error: ±10% @25 ℃, 5V
    ±20% @-40 ℃~105 ℃, 5V
  - Internal high-speed RC oscillator: 1MHz
  - External crystal oscillator: 32768Hz/4MHz
  - 8 resets, brown-out reset voltage (BOR): 2.8V/3.3V/3.7V/4.2V
  - Low voltage detection: 2.7V/3.0V/3.3V/3.6V/3.9V/4.2V
- **IO**
  - PB ports built-in pull-up resistors 28k, other IO ports built-in pull-up resistors 4.7k
  - High current sink port (PB0~PB7)
  - Support device peripheral function multiolexing
  - All IO ports support external interrupt function, INT0~2 external interrupt (rise-edge, falling-edge, double-edge) , INT3(rise-edge, falling-edge) share interrupt source
- **Communication module**
  - 2xUART communication, support I/O mapping
  - 1xIIC hardware slave, support 100/400kHz
- **16-bit PWM**
  - PWM0 supports 4 channels, which shares the period, duty cycle and polarity are configurable
  - PWM1/2 both support 1 channel output
- **Operating voltage: 2.7V~5.5V**
- **Operating temperature: -40 ℃~105 ℃**
  - Enhanced industrial grade, in line with JESD industrial grade reliability certification standard
- **12-bit high-precision ADC**
  - Up to 26 analog input channels
  - Reference voltage: VCC/2V/4V
- **Interrupt**
  - Two-level interrupt priority selectable
  - ADC, CSD, LED, INT0/1/2/3, LVDT, Timer0/1/2, WDT, UART0/1, IIC
- **Timer**
  - Three 16-bit Timer
  - Timer2 clock source: LIRC32k or XTAL 32768Hz/4MHz
  - Watchdog timer, overflow time 18ms to 2.304s
- **LED driver**
  - 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8 dot matrix driver
  - LED0~LED8 scan sequence is configurable
- **Low power mode**
  - Idle mode and sleep mode
  - Deep sleep, power consumption 7μA @5V
- **CTK**
  - The key sensitivity can be set independently
  - Capacitive keys can be reused as GPIO
- **Two-wire programming, single-wire debugging simulation interface**
- **Package**
  - SOP16/SOP20/SOP28

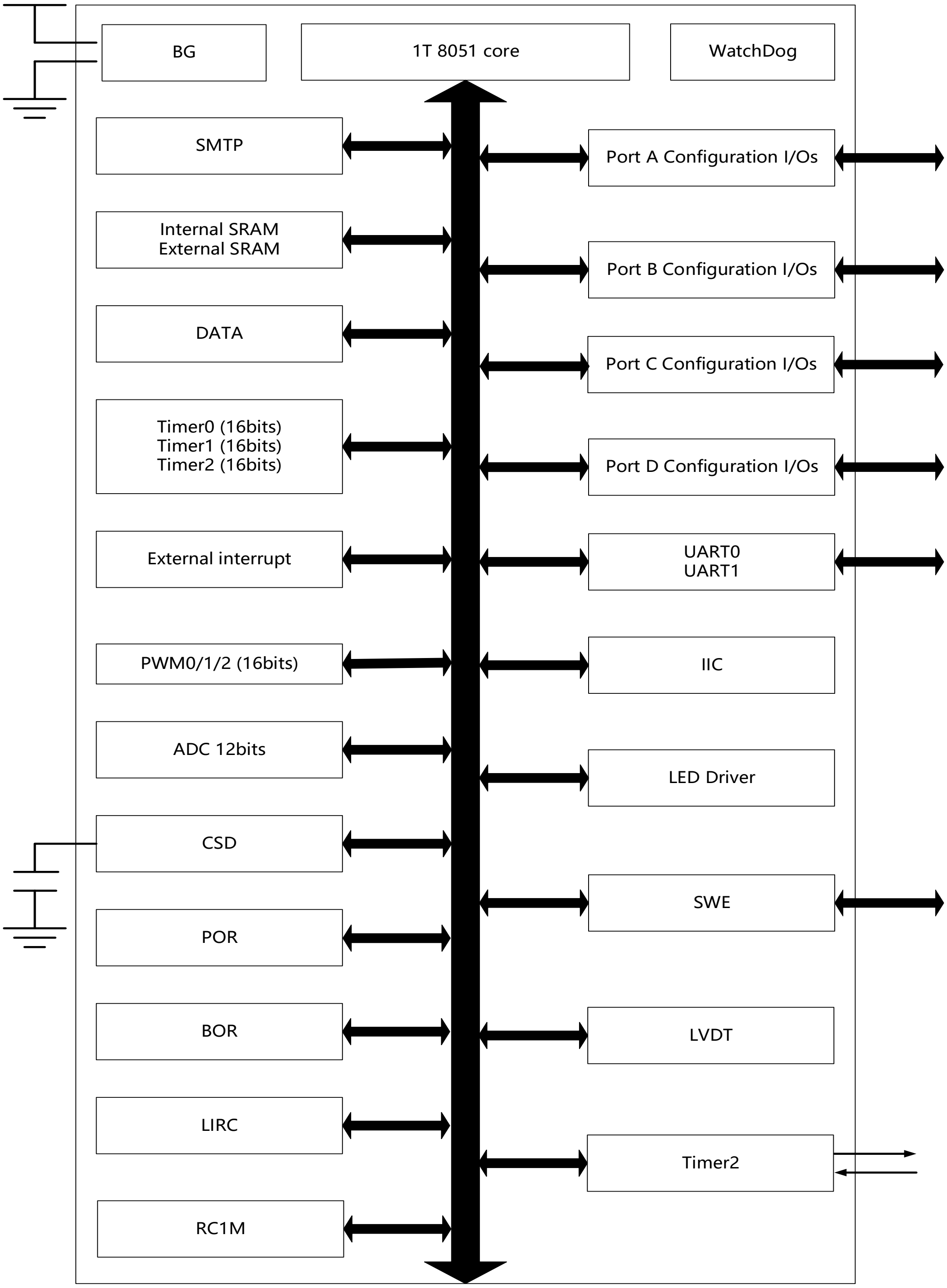
1.2. Overview

The BF7612DMXX-SJLX uses the high speed 8051 core with 1T instruction cycle, compared to the standard 8051 (12T) instruction cycle, it has the quicker running speed, compatibility standard 8051 instruction.

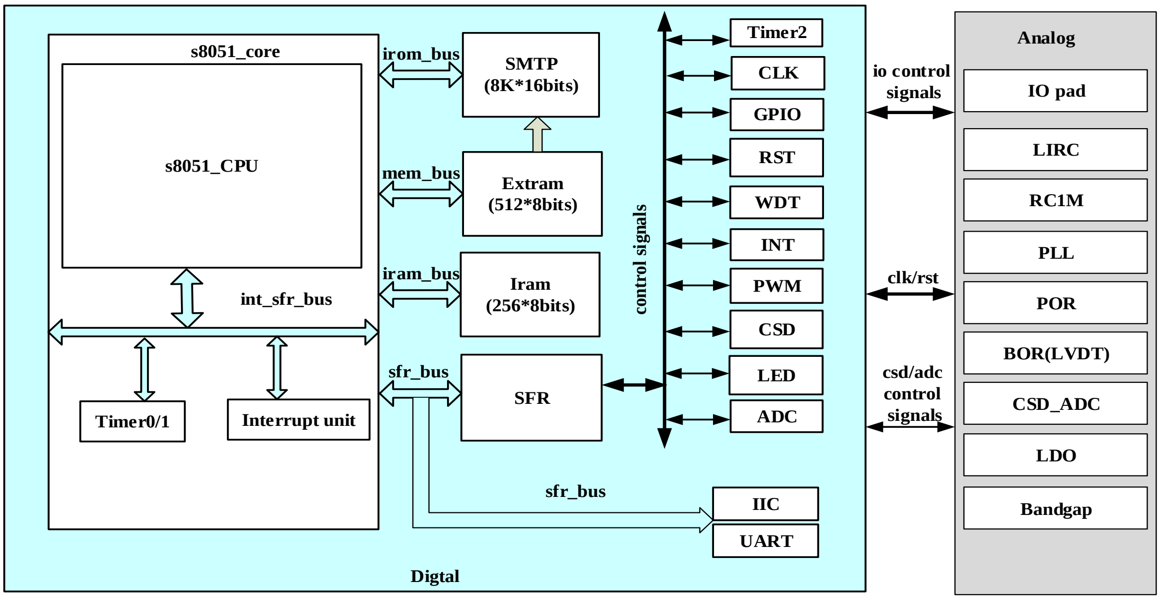
The BF7612DMXX-SJLX includes a watchdog, key detection, LED serial dot matrix driver, IIC, UART, low voltage detection, power down reset, three 16bit PWM, Timer0, Timer1, Timer2, 12bit successive approximation ADC, low power mode, etc.

The BF7612DMXX-SJLX integrated capacitance channels, which can be used to detect proximity sensing or touch, its built-in MCU, can be flexible configurated, through the configuration can be implemented keys, rollers, sliders and other applications. A key can be run independently, and each key can be adjusted by corresponding special function registers to adjust the sensitivity.

1.3. System Architecture

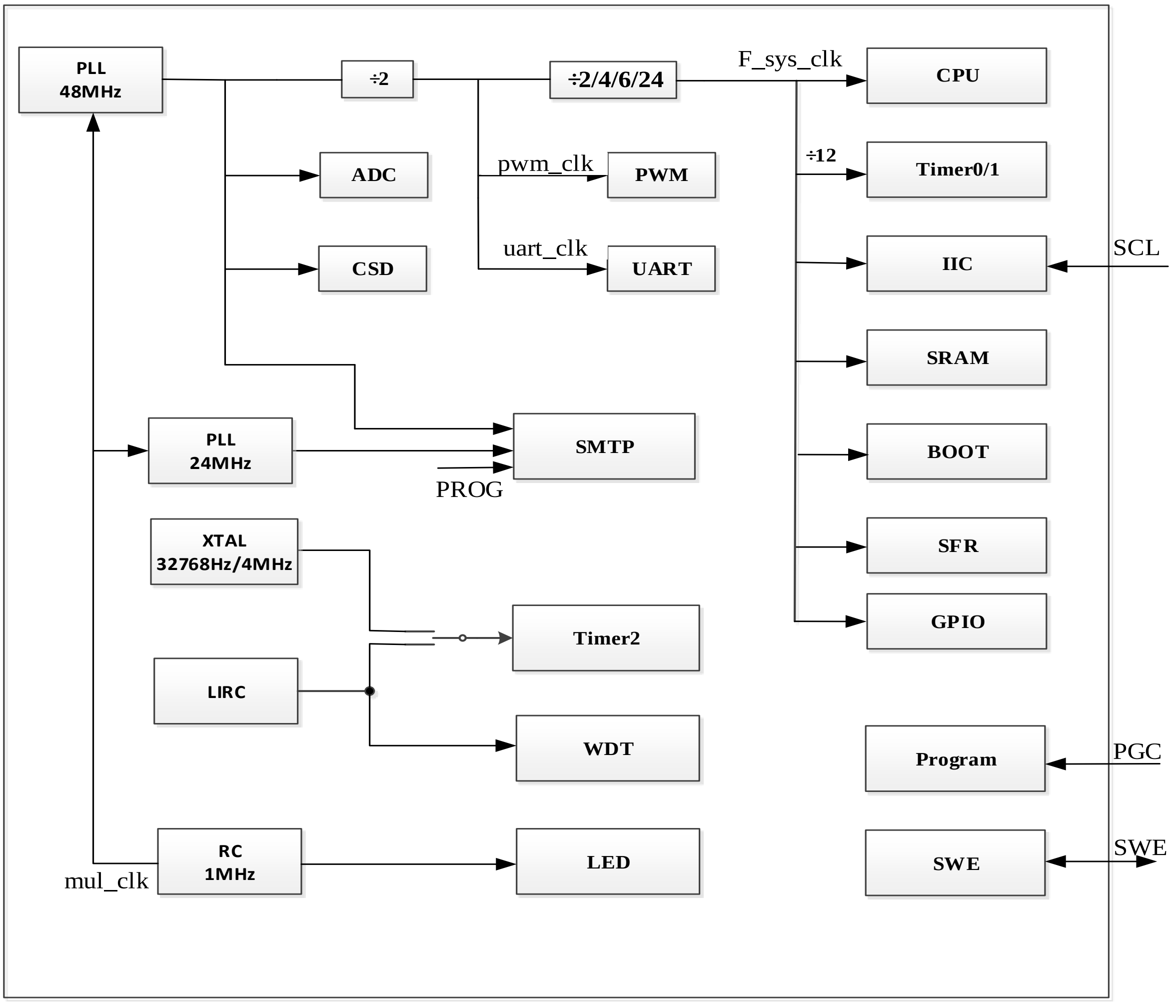


system architecture



system bus frame diagram

1.4. Clock Diagram



clock diagram

1.5. Selection List

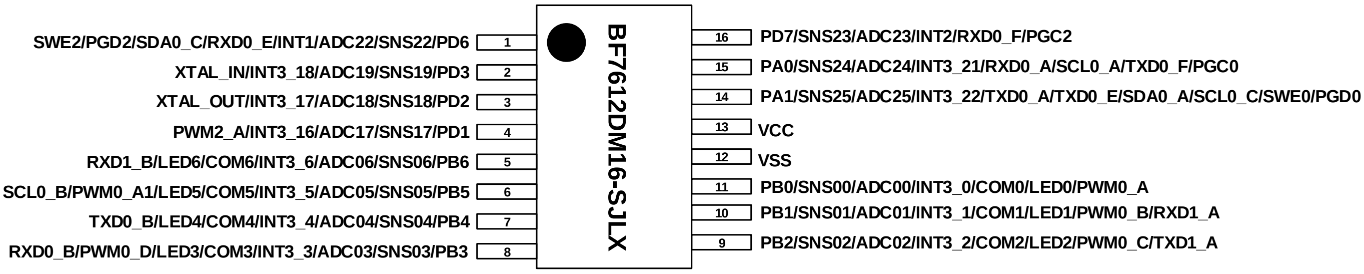
Type		BF7612DM16-SJLX	BF7612DM20-SJLX	BF7612DM28-SJLX
Operation voltage (V)		2.7~5.5	2.7~5.5	2.7~5.5
Operating frequency (Hz)		12M	12M	12M
Core		1T 8051	1T 8051	1T 8051
Memory (Bytes)	CODE	16/15/14/13/12K	16/15/14/13/12K	16/15/14/13/12K
	BOOT	0/1/2/3/4K	0/1/2/3/4K	0/1/2/3/4K
	DATA	1K	1K	1K
	SRAM	256+512	256+512	256+512
Timer	WDT	1	1	1
	Timer0*16bit	1	1	1
	Timer1*16bit	1	1	1
	Timer2*16bit	1	1	1
Communication module	IIC	1	1	1
	UART	2	2	2
GPIO		14	18	26
KEY		14	18	26
INT		14	18	26
COM		7	8	8
Analog module	ADC*12bit	14	18	26
Display module	LED serial	6*7	7*8	8*8
PWM module	PWM0*16bit	4	4	4
	PWM1*16bit	0	1	1
	PWM2*16bit	1	0	1
Package		SOP16(9.9*3.9mm)	SOP20(12.8*7.5mm)	SOP28(18*7.5mm)

Selection list

Note: CODE area + BOOT area space is 16 KB.

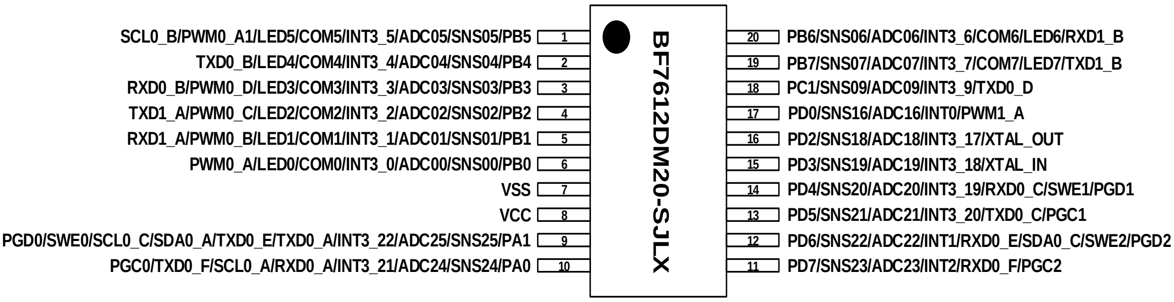
1.6. Pin Assignment

1.6.1. SOP16



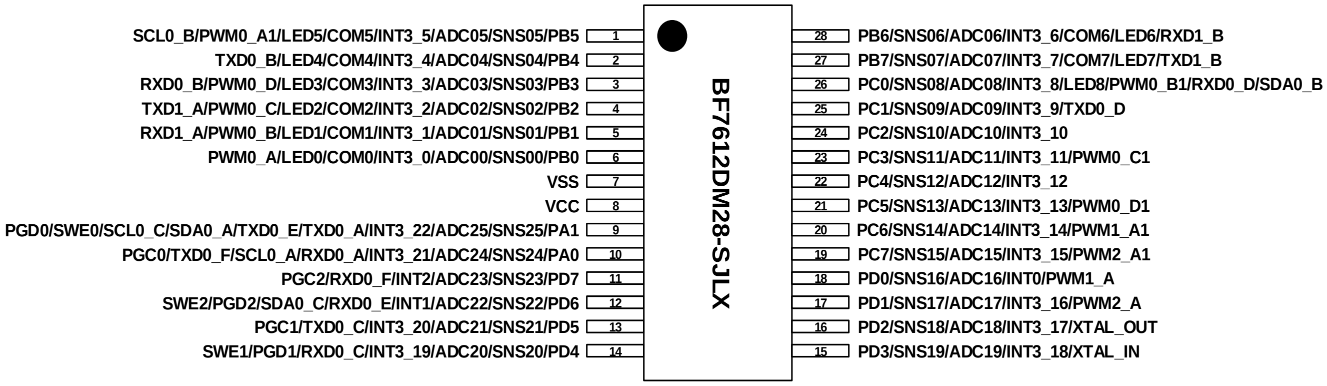
BF7612DM16-SJLX package pin diagram

1.6.2. SOP20



BF7612DM20-SJLX package pin diagram

1.6.3. SOP28



BF7612DM28-SJLX package pin diagram

1.7. Pin Description

BF7612DM28-SJLX	BF7612DM20-SJLX	BF7612DM16-SJLX	Function description
1	1	-	Default function: GPIO <PB5> Other function: SNS05: Touch key channel 05 ADC05: ADC channel 05 INT3_5: External Interrupt 3_5 COM5: Large sink current port LED5: LED serial dot matrix PWM0_A1: PWM0_A1 output port SCL0_B: Serial clock line of IIC
2	2	7	Default function: GPIO <PB4> Other function: SNS04: Touch key channel 04 ADC04: ADC channel 04 INT3_4: External Interrupt 3_4 COM4: Large sink current port LED4: LED serial dot matrix TXD0_B: Serial port transmitting
3	3	8	Default function: GPIO <PB3> Other function: SNS03: Touch key channel 03 ADC03: ADC channel 03 INT3_3: External Interrupt 3_3 COM3: Large sink current port LED3: LED serial dot matrix PWM0_D: PWM0_D output port RXD0_B: Serial port receiving
4	4	9	Default function: GPIO <PB2> Other function: SNS02: Touch key channel 02 ADC02: ADC channel 02 INT3_2: External Interrupt 3_2 COM2: Large sink current port LED2: LED serial dot matrix PWM0_C: PWM0_C output port TXD1_A: Serial port transmitting

5	5	10	Default function: GPIO <PB1> Other function: SNS01: Touch key channel 01 ADC01: ADC channel 01 INT3_1: External Interrupt 3_1 COM1: Large sink current port LED1: LED serial dot matrix PWM0_B: PWM0_B output port RXD1_A: Serial port receiving
6	6	11	Default function: GPIO <PB0> Other function: SNS0: Touch key channel 00 ADC00: ADC channel 00 INT3_0: External Interrupt 3_0 COM0: Large sink current port LED0: LED serial dot matrix PWM0_A: PWM0_A output port
7	7	12	Default function: GND <VSS>
8	8	13	Default function: Power supply <VCC>
9	9	14	Default function: GPIO <PA1> Other function: SNS25: Touch key channel 25 ADC25: ADC channel 25 INT3_22: External Interrupt 3_22 SDA0_A: Serial data line of IIC TXD0_A: Serial port transmitting TXD0_E: Serial port transmitting SCL0_C: Serial clock line of IIC SWE0: Single-line simulation PGD0: Programming port
10	10	15	Default function: GPIO <PA0> Other function: SNS24: Touch key channel 24 ADC24: ADC channel 24 INT3_21: External Interrupt 3_21 RXD0_A: Serial port receiving TXD0_F: Serial port transmitting SCL0_A: Serial clock line of IIC PGC0: Programming port
11	11	16	Default function: GPIO <PD7> Other function: SNS23: Touch key channel 23 ADC23: ADC channel 23 INT2: External Interrupt 2 RXD_F: Serial port receiving PGC2: Programming port

12	12	1	Default function: GPIO <PD6> Other function: SNS22: Touch key channel 22 ADC22: ADC channel 22 INT1: External Interrupt 1 SDA0_C: Serial data line of IIC RXD0_E: Serial port receiving PGC2: Programming port SWE2: Single-line simulation
13	13	-	Default function: GPIO <PD5> Other function: SNS21: Touch key channel 21 ADC21: ADC channel 21 INT3_20: External Interrupt 3_20 TXD0_C: Serial port transmitting PGC1: Programming port
14	14	-	Default function: GPIO <PD4> Other function: SNS20: Touch key channel 20 ADC20: ADC channel 20 INT3_19: External Interrupt 3_19 RXD0_C: Serial port receiving PGD1: Programming port SWE1: Single-line simulation
15	15	2	Default function: GPIO <PD3> Other function: SNS19: Touch key channel 19 ADC19: ADC channel 19 INT3_18: External Interrupt 3_18 XTAL_IN: External crystal input
16	16	3	Default function: GPIO <PD2> Other function: SNS18: Touch key channel 18 ADC18: ADC channel 18 INT3_17: External Interrupt 3_17 XTAL_OUT: External crystal output
17	-	4	Default function: GPIO <PD1> Other function: SNS17: Touch key channel 17 ADC17: ADC channel 17 INT3_16: External Interrupt 3_16 PWM2_A: PWM2_A output port
18	17	-	Default function: GPIO <PD0> Other function: SNS16: Touch key channel 16 ADC16: ADC channel 16 INT0: External Interrupt 0 PWM1_A: PWM1_A output port

19	-	-	Default function: GPIO <PC7> Other function: SNS15: Touch key channel 15 ADC15: ADC channel 15 INT3_15: External Interrupt 3_15 PWM2_A1: PWM2_A1 output port
20	-	-	Default function: GPIO <PC6> Other function: SNS14: Touch key channel 14 ADC14: ADC channel 14 INT3_14: External Interrupt 3_14 PWM1_A1: PWM1_A1 output port
21	-	-	Default function: GPIO <PC5> Other function: SNS13: Touch key channel 13 ADC13: ADC channel 13 INT3_13: External Interrupt 3_13 PWM0_D1: PWM0_D1 output port
22	-	-	Default function: GPIO <PC4> Other function: SNS12: Touch key channel 12 ADC12: ADC channel 12 INT3_12: External Interrupt 3_12
23	-	-	Default function: GPIO <PC3> Other function: SNS11: Touch key channel 11 ADC11: ADC channel 11 INT3_11: External Interrupt 3_11 PWM0_C1: PWM0_C1 output port
24	-	-	Default function: GPIO <PC2> Other function: SNS10: Touch key channel 10 ADC10: ADC channel 10 INT3_10: External Interrupt 3_10
25	18	-	Default function: GPIO <PC1> Other function: SNS09: Touch key channel 09 ADC09: ADC channel 09 INT3_9: External Interrupt 3_9 TXD0_D: Serial port transmitting
26	-	-	Default function: GPIO <PC0> Other function: SNS08: Touch key channel 08 ADC08: ADC channel 08 INT3_8: External Interrupt 3_8 LED8: LED serial dot matrix PWM0_B1: PWM0_B1 output port SDA0_B: Serial data line of IIC RXD0_D: Serial port receiving

27	19	-	Default function: GPIO <PB7> Other function: SNS7: Touch key channel 07 ADC07: ADC channel 07 INT3_7: External Interrupt 3_7 COM7: Large sink current port LED7: LED serial dot matrix TXD1_B: Serial port transmitting
28	20	5	Default function: GPIO <PB6> Other function: SNS6: Touch key channel 06 ADC06: ADC channel 06 INT3_6: External Interrupt 3_6 COM6: Large sink current port LED6: LED serial dot matrix RXD1_B: Serial port receiving

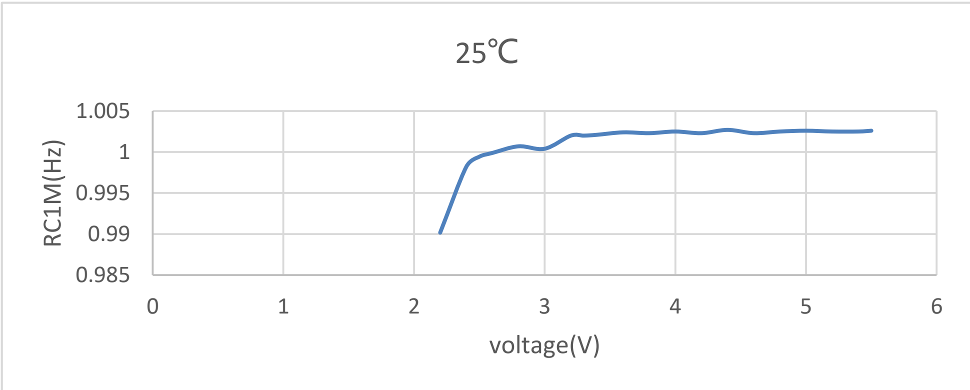
Package pin correspondence diagram

2. Electrical Characteristic

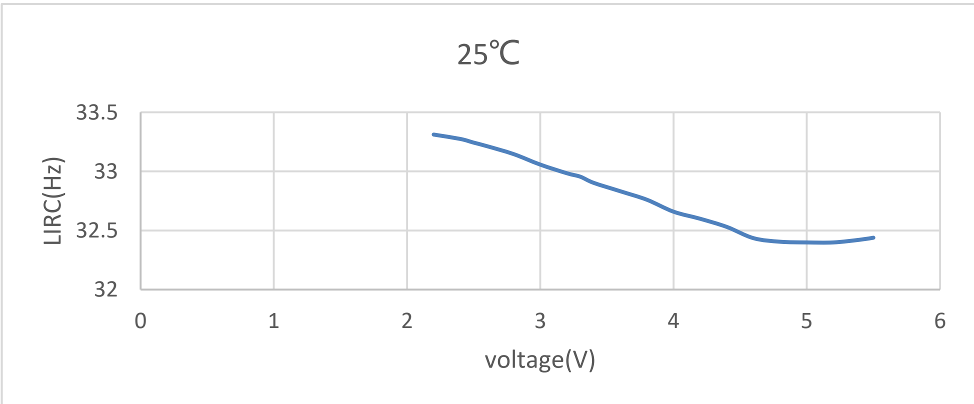
2.1. AC Characteristic

Parameter	Symbol	Conditions	Clock Error	Unit
RC	RC1M	Ambient temperature 25 ℃, @5V	±1%	MHz
		Ambient temperature -20 ℃ ~ 65 ℃, @5V	±1%	
		Ambient temperature -40 ℃ ~ 105 ℃, @5V	±3%	
		VCC 2.7V~5.5V, ambient temperature 25 ℃	±3%	
System clock	F_sys_clk	Ambient temperature 25 ℃, @5V	±1%	
		Ambient temperature -20 ℃ ~ 65 ℃, @5V	±1%	
		Ambient temperature -40 ℃ ~ 105 ℃, @5V	±3%	
		VCC 2.7V~5.5V, ambient temperature 25 ℃	±3%	
WDT clock	LIRC	Ambient temperature 25 ℃, @5V	±10%	kHz
		Ambient temperature -40 ℃ ~ 105 ℃, @5V	±20%	
		VCC 2.7V~5.5V, ambient temperature 25 ℃	±35%	

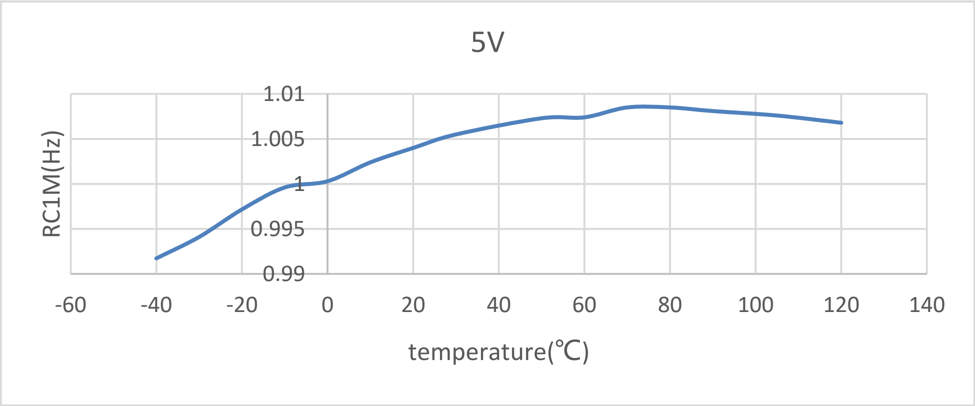
AC characteristic parameter table



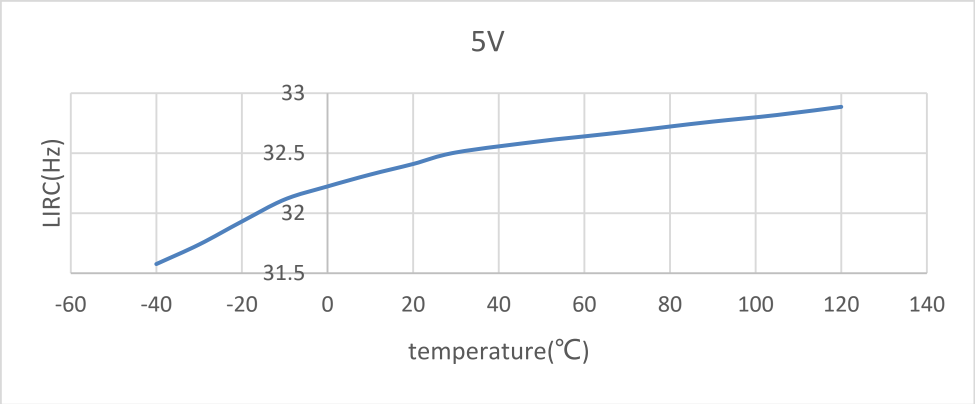
RC1M voltage curve



LIRC voltage curve



RC1M temperature curve



LIRC temperature curve

2.2. DC Characteristic

Unless otherwise stated, typical values are test values at 25℃ conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	VCC	-	2.7	-	5.5	V
Worek mode	Active	@5V, system clock 12M, no load, turn off other functions	-	3.2	4.2	mA
		@5V, system clock 6M, no load, turn off other functions	-	2.5	3.3	mA
		@5V, system clock 4M, no load, turn off other functions	-	2.3	3.0	mA
		@5V, system clock 1M, no load, turn off other functions	-	2	2.6	mA
		@3.3V, system clock 12M, no load, turn off other functions	-	3	3.9	mA
		@3.3V, system clock 6M, no load, turn off other functions	-	2.4	3.1	mA
		@3.3V, system clock 4M, no load, turn off other functions	-	2.2	2.9	mA
		@3.3V, system clock 1M, no load, turn off other functions	-	1.9	2.5	mA
	Wait	@5V, system clock 12M, IO output is low, enter Wait mode, turn off all other functions	-	1.8	2.3	mA
		@3.3V, system clock 12M, IO output is low, enter Wait mode, turn off all other functions	-	1.7	2.2	mA
	Idle	@5V, WDT_CTRL=7, WDT interrupt 2s wake up, 2ms work time, IO output is low, turn off all other functions	-	10.2	13.3	μA
		@5V, Timer2 external crystal oscillator 2s wake up, 2ms work time, IO output is low, turn off all other functions	-	10.2	13.3	μA
		@3.3V, WDT_CTRL=7, WDT interrupt 2s wake up, 2ms work time, IO output is low, turn off all other functions	-	8.0	10.4	μA
		@3.3V, Timer2 external crystal oscillator 2s wake up, 2ms work time, IO output is low, turn off all other functions	-	8.0	10.4	μA
		@5V, CSD parallel mode, WDT interrupt 2S wake up, 2ms working time, IO output is low, turn off all other functions	-	10.2	13.3	μA
		@3.3V, CSD parallel mode, WDT interrupt 2S wake up, 2ms working time, IO output is low, turn off all other functions	-	8.0	10.4	μA
	Sleep	@5V PCON = 0x01, close BOR, IO set to low, turn off all other functions	-	7.0	9.1	μA
		@3.3V PCON = 0x01, close BOR, IO set to low, turn off all other functions	-	5.0	6.5	μA
Input low level	V_{IL}	VCC=2.7~5.5V	-	-	0.3*VCC	V
Input ligh level	V_{IH}	VCC=2.7~5.5V	0.7*VCC	-	-	V
INT0/1/2/3 input low level	V_{INTL}	VCC=2.7~5.5V	-	-	0.3*VCC	V
INT0/1/2/3 input high level	V_{INTH}	VCC=2.7~5.5V	0.7*VCC	-	-	V

Output low level	V_{OL}	IOL=4mA@VCC=2.7V, IOL=10mA@VCC=5V	-	-	0.1*VCC	V
Output high level	V_{OH}	IOH=4mA@VCC=2.7V, IOH=10mA@VCC=5V	0.9VCC	-	-	V
IO sink current	IOL	V_{OL} =0.1VCC, @VCC=5V	48.0	68	88.4	mA
IO source current	IOH	V_{OH} =0.9VCC, @VCC=5V	13.0	18.5	24.0	mA
PB large sink current	I_{COM}	V_{OL} =0.1VCC, @VCC=5V	84	120	156	mA
Input leakage current	I_{Le}	VCC=5V	-	0.5	1	μA
IO pull-up resistors	R_{P_u}	VCC=5V	3.3	4.7	6.1	kΩ
PB pull-up resistors	R_{P_u}	VCC=5V	19.6	28	36.4	kΩ
PB pull-down resistors	R_{P_d}	VCC=5V	19.6	28	36.4	kΩ

The working current of the functional module is shown in the following table:

Module	Symbol	**Conditions**	**Min**	**Typical**	**Max**	**Unit**
ADC working current	I_{ADC}	@5V, system clock 12M, no load, IO output is low, enable ADC, open a channel, GET_ADC scan, turn off all other functions	-	0.5	-	μA
LVDT working current	I_{LVDT}	@5V, system clock 12M, no load, in low-power mode, IO output is low. The LVDT function is enabled, and all other functions are disabled	-	7.2	-	μA
BOR working current	I_{BOR}	@5V, system clock 12M, no load, In low-power mode, the IO output is low. The BOR function is enabled, and all other functions are disabled	-	7.0	-	μA
CSD working current	I_{CSD}	@5V, system clock 12M, no load, IO output low, open CSD six channels and Timer0, turn off all other functions	-	0.38	-	mA
PWM working current	I_{PWM}	@5V, system clock 12M, no load, low IO output, enable PWM0, initialize 4K, disable all other functions	-	0.15	-	mA
DATA wipe current	$I_{\_E}$	@5V, system clock 12M, no load, low IO output, enable DATA, erase DATA in while, disable all other functions	-	2.6	-	mA
DATA write current	$I_{\_W}$	@5V, system clock 12M, no load, low IO output, enable DATA, write only one byte in while, disable all other functions	-	2.0	-	mA

DC characteristics parameters table

2.3. ADC Characteristic

Unless otherwise stated, typical values are test values at 25℃ conditions.

ADC Electrical Characteristics VDD=Vmin-5.5V, GND=0V, T_A=+25 ℃						
Parameter	**Symbol**	**Conditions**	**Min**	**Typical**	**Max**	**Unit**
Supply voltage	V_{AD}	-	2.7	-	5.5	V
Accuracy	N_R	-	-	9	10	Bit
A/D input voltage	VAIN	-	VSS	-	V_{REF}	V
A/D input resistance	R_{AIN}	VCC=5V, RC filtering	-	12	-	kΩ
		VCC=5V, no RC filtering	-	2.3	-	kΩ
A/D work current	I_{AD}	-	-	0.5	-	mA
A/D input current	I_{ADIN}	-	-	-	1	μA
Differential nonlinear error	D_{LE}	VDD=5.0V	-	±4	±6	LSB
Integral nonlinear error	L_{LE}	VDD=5.0V	-	±4	±6	LSB
ADC sample time	T_{AD}	-	1.3	-	-	μs
ADC conversion time	TCON	-	7.87	-	-	μs
Resolution	ADCRESO	-	12			Bit
Input channel	-	-	-	-	26	Channel

ADC characteristic parameter table

2.4. Limit Parameter

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage when working	VCC	VSS+2.7	-	VSS+5.5	V
Non-working storage temperature	Tstg	-40	-	125	℃
Operating temperature	Totg	-40	-	105	℃
I/O input voltage	Vin	VSS-0.5	-	VCC+0.5	V
IOL total current	IOLA	130			mA
IOH total current	IOHA	-130			mA
Port electrostatic discharge voltage	ESD(HBM)	-6	-	6	kV

Limit parameters characteristics parameters table

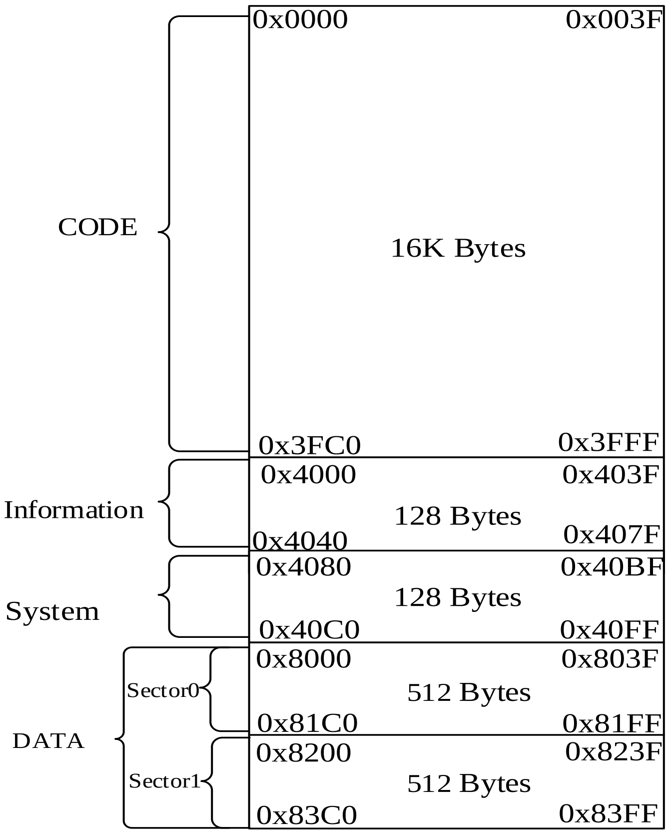
Notes: Exceed the limit parameters may cause damage to the chip, unable to expect the chip work outside the above indicated range. If you work under conditions outside the marked range for a long time, it may affect the reliability of the chip.

3. Memory and SFR

3.1. SMTP

SMTP features are as follows:

- CODE area: ICP programming supports block erasing, page erasing and word writing
- DATA area: Support block erasing, sector erasing, page erasing, and word writing
- Program/erase time: CODE area: at least 10000 times @25℃
  DATA area: at least 10000 times @25℃
- Data retention period: 100 years @25℃
  10 years @85℃
- Support IAP BOOT upgrade function, BOOT area size is 1/2/3/4K



Address allocation structure diagram

Module	Size of space(bytes)	Address	Page
CODE	16K	0x0000~0x3FFF	128
Information	128	0x4000~0x407F	1
System	128	0x4080~0x40FF	1
DATA	1K	0x8000~0x83FF	8

Note: Each page size is 128 Bytes

Steps for reading chip unique identifier (UID):

1. Turn off interrupt;
2. The absolute CODE addresses 0x402E to 0x403D correspond to product ID1 to ID16;
3. Restore the interrupt setting;

3.2. RAM

There are 256 Bytes inside, with addresses ranging from 00H to FFH. These include the working register group, bit-addressing area, buffer, and SFR, where the buffer contains the stack area.

Internal low 128 Bytes: a total of 128 Bytes from 00H to 7FH. Data can be read and written in either immediate or indirect addressing mode.

Internal high 128 Bytes: a total of 128 Bytes from 80H to FFH. Data can only be read and written through the working register indirect addressing mode.

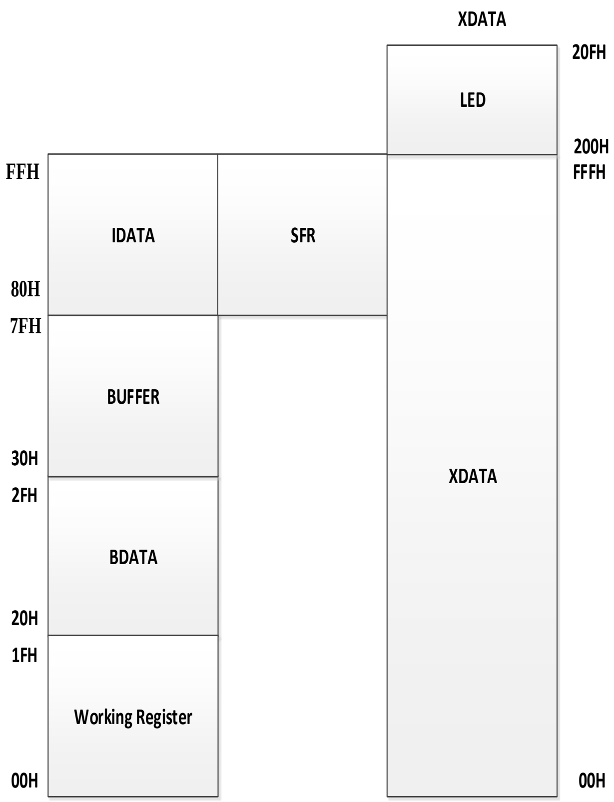
Special function register SFR: Address is 80H~FFH, can only read and write data by direct addressing.

Xdata contains 512 Bytes. The address ranges from 0000H to 01FFH. Users can use this area completely. Data is read and written by means of data pointers or working register addressing.

LED storage RAM occupies XRAM bus, Address is 200~20FH. This area is the LED display cache, and the display content can be modified by changing the data in this area.

When writing programs, pay attention to reserving stack space to avoid the program running out of stack overflow. In C programming, the stack header is automatically assigned by the program, but must be stored in data or IDATA. The start address of the stack can be set in startup. A51 in Keil.

RAM address space allocation diagram:



RAM	(MSB)							(LSB)	
7FH									Buffer
2FH	7F	7E	7D	7C	7B	7A	79	78	Bit addressing area
2EH	77	76	75	74	73	72	71	70	
2DH	6F	6E	6D	6C	6B	6A	69	68	
2CH	67	66	65	64	63	62	61	60	
2BH	5F	5E	5D	5C	5B	5A	59	58	
2AH	57	56	55	54	53	52	51	50	
29H	4F	4E	4D	4C	4B	4A	49	48	
28H	47	46	45	44	43	42	41	40	
27H	3F	3E	3D	3C	3B	3A	39	38	
26H	37	36	35	34	33	32	31	30	
25H	2F	2E	2D	2C	2B	2A	29	28	
24H	27	26	25	24	23	22	21	20	
23H	1F	1E	1D	1C	1B	1A	19	18	
22H	17	16	15	14	13	12	11	10	
21H	0F	0E	0D	0C	0B	0A	09	08	
20H	07	06	05	04	03	02	01	00	
1FH 18H	3 groups								Working register area
17H 10H	2 groups								
0FH 08H	1 groups								
07H 00H	0 groups								

address allocation map for each bit addressing area

The following table lists the methods to get value in the three parts of RAM:

DATA	MOV A,direct
	MOV direct,A
	MOV direct,#data
	MOV direct1,direct2
	MOV Rn,direct
	MOV direct,Rn

IDATA	MOV A,@Ri
	MOV @Ri,A
	MOV direct,@Ri
	MOV @Ri,direct
	MOV @Ri,#data

XDATA	MOVX @DPTR,A MOVX A,@DPTR

RAM value instruction table

In the above table, n ranges from 0 to 7, and i ranges from 0 to 1.

3.3. SFR Table

Address	Name	RW	Reset value	Description
0x80	DATAB	RW	1111_1111b	PB data register
0x81	SP	RW	0000_0111b	Stack pointer register
0x82	DPL	RW	0000_0000b	Data pointer register 0 low 8 bits
0x83	DPH	RW	0000_0000b	Data pointer register 0 high 8 bits
0x84	SYS_CLK_CFG	RW	xxxx_x001b	Clock control register
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT power-on/brown-out interrupt status register
0x87	PCON	RW	xxxx_xxx0b	Low-power mode select register
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bits
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bits
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bits
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8 bits
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0x90	DATAC	RW	1111_1111b	PC port data register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow configuration register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable configuration register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 count value configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 count value configuration register, low 8 bits
0x96	REG_ADDR	RW	xx00_0000b	Second address bus register
0x97	REG_DATA	RW	0000_0000b	Second data read and write bus register
0x98	DATAD	RW	1111_1111b	PD data register
0x99	PWM1_L_L	RW	0000_0000b	PWM1 low level control register (low 8 bits)
0x9A	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8 bits)
0x9B	PWM1_H_L	RW	0000_0000b	PWM1 high level control register (low 8 bits)

0x9C	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8 bits)
0x9D	PWM2_L_L	RW	0000_0000b	PWM2 low level control register (low 8 bits)
0x9E	PWM2_L_H	RW	0000_0000b	PWM2 low level control register (high 8 bits)
0x9F	PWM2_H_L	RW	0000_0000b	PWM2 high level control register (low 8 bits)
0xA0	P2_XH	RW	1111_1111b	MOVX @Ri, A operation pdata address high 8 bits
0xA1	PWM2_H_H	RW	0000_0000b	PWM2 high level control register (high 8 bits)
0xA2	PWM_EN	RW	xxx0_0000b	PWM control register
0xA3	PWM0_CH_CTRL	RW	0000_0000b	PWM0 control register
0xA4	PWM0_CH0_CNT_L	RW	0000_0000b	PWM0 channel 0 count value configuration register(low 8 bits)
0xA5	PWM0_CH0_CNT_H	RW	0000_0000b	PWM0 channel 0 count value configuration register(high 8 bits)
0xA6	PWM0_CH1_CNT_L	RW	0000_0000b	PWM0 channel 1 count value configuration register(low 8 bits)
0xA7	PWM0_CH1_CNT_H	RW	0000_0000b	PWM0 channel 1 count value configuration register(high 8 bits)
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register 0
0xA9	PWM0_CH2_CNT_L	RW	0000_0000b	PWM0 channel 2 count value configuration register(low 8 bits)
0xAA	PWM0_CH2_CNT_H	RW	0000_0000b	PWM0 channel 2 count value configuration register(high 8 bits)
0xAB	PWM0_CH3_CNT_L	RW	0000_0000b	PWM0 channel 3 count value configuration register(low 8 bits)
0xAC	PWM0_CH3_CNT_H	RW	0000_0000b	PWM0 channel 3 count value configuration register(high 8 bits)
0xAD	PWM0_MOD_L	RW	0000_0000b	PWM0 period configuration register (low 8 bits)
0xAE	PWM0_MOD_H	RW	0000_0000b	PWM0 period configuration register (high 8 bits)
0xAF	SCAN_START	RW	xxxx_xxx0b	LED scan open register
0xB0	DP_CON	RW	xxx0_0000b	LED scan control register
0xB1	SCAN_WIDTH	RW	0000_0000b	LED scan turn-on time 1 control register
0xB2	LED2_WIDTH	RW	0000_0000b	LED scan turn-on time 2 control

				register
0xB3	LED_DRIVE	RW	xxxx_0000b	LED driver capability configuration register
0xB4	ADC_SPT	RW	0000_0000b	ADC sample time configuration register
0xB5	ADC_SCAN_CFG	RW	xx00_0000b	ADC scan control register
0xB6	ADCCKC	RW	xxxx_xx00b	ADC clock control register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xB9	ADC_RDATAH	R	xxxx_0000b	ADC scan result register high 4 bits
0xBA	ADC_RDATAL	R	0000_0000b	ADC scan result register low 8 bits
0xBB	ADC_CFG1	RW	0000_0000b	ADC sample timing control register 1
0xBC	ADC_CFG2	RW	x000_111xb	ADC sample timing control register 2
0xBD	UART0_BDL	RW	0000_0000b	UART0 baudrate control register
0xBE	UART0_CON1	RW	x000_0000b	UART0 control register 1
0xBF	UART0_CON2	RW	xxxx_1100b	UART0 control register 2
0xC0	UART0_STATE	R/RW	x000_0000b	UART0 status flag register
0xC1	UART0_BUF	RW	1111_1111b	UART0 data register
0xC2	UART_IO_CTRL	RW	xxxx_xx00b	UART pin exchange register
0xC3	UART_IO_CTRL1	RW	xxxx_0000b	UART pin enable register
0xC4	LED_IO_START	RW	xxxx_0000b	LED start port control register
0xC5	UART1_BDL	RW	0000_0000b	UART1 baudrate control register
0xC6	UART1_CON1	RW	x000_0000b	UART1 control register 1
0xC7	UART1_CON2	RW	xxxx_1100b	UART1 control register 2
0xC8	UART1_STATE	R/RW	x000_0000b	UART1 status flag register
0xC9	UART1_BUF	RW	1111_1111b	UART1 data register
0xCA	CSD_START	RW	xxxx_xxx0b	CSD scan open register
0xCB	SNS_SCAN_CFG1	RW	x000_0000b	Touch key scan configuration register 1
0xCC	SNS_SCAN_CFG2	RW	x100_0000b	Touch key scan configuration register 2
0xCD	SNS_SCAN_CFG3	RW	x111_0000b	Touch key scan configuration register 3
0xCE	CSD_RAWDATAL	R	0000_0000b	CSD count value low 8 bits
0xCF	CSD_RAWDATAH	R	0000_0000b	CSD count value high 8 bits
0xD0	PSW	R/RW	0000_0000b	Program status word register
0xD1	PULL_I_SELA_L	RW	0000_0000b	CSD pull-up current source

				selection register
0xD2	SNS_ANA_CFG	RW	xx10_1111b	CSD scan parameter configuration register
0xD3	SNS_IO_SEL1	RW	0000_0000b	SNS channel selection register 1
0xD4	SNS_IO_SEL2	RW	0000_0000b	SNS channel selection register 2
0xD5	SNS_IO_SEL3	RW	0000_0000b	SNS channel selection register 3
0xD6	SNS_IO_SEL4	RW	xxxx_xx00b	SNS channel selection register 4
0xD7	RST_STAT	RW	0000_0010b①	Reset flag register
0xD8	PD_PB	RW	0000_0000b	PB port pull-down resistance control register
0xD9	ADC_IO_SEL1	RW	0000_0000b	ADC function select register 1
0xDA	ADC_IO_SEL2	RW	0000_0000b	ADC function select register 2
0xDB	ADC_IO_SEL3	RW	0000_0000b	ADC function select register 3
0xDC	ADC_IO_SEL4	RW	xxxx_xx00b	ADC function select register 4
0xDD	PU_PA	RW	xxxx_xx00b	PA port pull-up resistance enable register
0xDE	PU_PB	RW	0000_0000b	PB port pull-up resistance enable register
0xDF	PU_PC	RW	0000_0000b	PC port pull-up resistance enable register
0xE0	ACC	RW	0000_0000b	Accumulator
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE2	PU_PD	RW	0000_0000b	PD port pull-up resistance enable register
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit and receive data register
0xE5	IICCON	RW	xx01_0000b	IIC control register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xEA	TRISA	RW	xxxx_xx11b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_1111b	PC direction register
0xED	TRISD	RW	1111_1111b	PD direction register
0xEE	COM_IO_SEL	RW	0000_0000b	COM port select configuration register
0xEF	ODRAIN_EN	RW	xxxx_x000b	PA0/PA1/PD6 open leakage

				output enable register
0xF0	B	RW	0000_0000b	B register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x10x_x000b	IIC/INT function control register
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	EXT_INT_CON	RW	x001_0101b	External interrupt polarity control register
0xF8	DATAA	RW	xxxx_xx11b	PA data register
0xF9	SPROG_ADDR_H	RW	0x00_0000b	Address control register high 8 bits
0xFA	SPROG_ADDR_L	RW	0000_0000b	Address control register low 8 bits
0xFB	SPROG_DATA	RW	0000_0000b	Data register
0xFC	SPROG_CMD	RW	0000_0000b	Command register
0xFD	SPROG_TIM	RW	1001_1010b	Erase time control register
0xFE	PD_ANA	RW	xxx1_0111b	Module switch control register
0xFF	BOR_LVDT_VTH	RW	xx00_0000b	BOR and LVDT threshold selection register

SFR register summary table

Note:

1. **Registers whose addresses end with 8 or 0 can be bit-operated, such as 0x80, 0x88 register address.**
2. **Reset value: Reset values of different modes(8 reset modes, watchdog timer overflow reset, power-on reset reset, brown-out reset, programming reset,tuning configuration reset, PC pointer overflow reset, oftware reset, BOOT address jump reset).**
3. **'①' is reset to 1 after power-on. Other resets: Reset to 0 after power-on and 1 after corresponding reset.**
4. **R: Only read; RW: Read and write.**
5. **'x': Indeterminate state.**
6. **The reserved registers and the reserved bits of the registers are forbidden to write operation, otherwise it may cause the chip abnormality.**

3.4. Secondary Bus Register Table

The BF7612DMXX-SJLX series support expanded secondary bus registers for expanding more register functions. Just write the address of the secondary bus register to be accessed into REG_ADDR, and then access the corresponding secondary bus register through the REG_DATA register. It is recommended that when reading and writing secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed. Prevent other interrupts or operations from modifying the address or data of the secondary bus register.

Secondary bus					
Address	**Name**	**Bit**	**RW**	**Description**	**Reset value**
0x96	REG_ADDR	<5:0>	RW	Secondary bus address configuration register	0x00
0x97	REG_DATA	<7:0>	RW	Second data read and write bus register	0x00

Address	Name	RW	Reset value	Description
0x00	CFG0_REG	R	1111_1111b①	Configuration word register 0
0x01	CFG1_REG	R	0000_0001b①	Configuration word register 1
0x02	CFG2_REG	R	0001_1101b①	Configuration word register 2
0x03	CFG3_REG	R	0011_1111b①	Configuration word register 3
0x04	CFG4_REG	R	1100_1001b①	Configuration word register 4
0x05	CFG5_REG	R	1100_1101b①	Configuration word register 5
0x06	CFG6_REG	R	1111_1111b①	Configuration word register 6
0x07	CFG7_REG	R	0011_1111b①	Configuration word register 7
0x08	CFG8_REG	R	0110_0100b①	Configuration word register 8
0x09	CFG9_REG	R	0111_1111b①	Configuration word register 9
0x0A	CFG10_REG	R	0000_1111b①	Configuration word register 10
0x0B	CFG11_REG	R	1111_1111b①	Configuration word register 11
0x0C	CFG12_REG	R	0000_0111b①	Configuration word register 12
0x0D	CFG13_REG	R	0000_0011b①	Configuration word register 13
0x0E	CFG14_REG	R	1111_1111b①	Configuration word register 14
0x0F	CFG15_REG	R	1111_1111b①	Configuration word register 15
0x10	CFG16_REG	R	1111_1111b①	Configuration word register 16
0x11	CFG17_REG	R	0000_0011b①	Configuration word register 17
0x12	CFG18_REG	R	1111_1111b①	Configuration word register 18
0x13	CFG19_REG	R	1111_1111b①	Configuration word register 19
0x14	CFG20_REG	R	1111_1111b①	Configuration word register 20
0x15	CFG21_REG	R	0010_1010b①	Configuration word register 21
0x16	CFG22_REG	R	0000_0001b①	Configuration word register 22
0x17	CFG31_REG	R	0000_0111b①	Configuration word register 31
0x1A	CFG30_REG	R	1111_1111b①	Configuration word register 30

0x20	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal clock selection register
0x21	BOOT_CMD	RW	0000_0000b	Program space jump instruction register
0x22	ROM_OFFSET_L	R	0000_0000b	Address offset of CODE area, low 8 bit
0x23	ROM_OFFSET_H	R	0000_0000b	Address offset of CODE area, high 8 bit
0x24	BOOT_EN	R	xxxx_xxx0b	BOOT mode status register
0x25	PERIPH_IO_SEL3	RW	x000_0000b	INT3 select enable register 3
0x26	PERIPH_IO_SEL2	RW	0000_0000b	INT3 select enable register 2
0x27	PERIPH_IO_SEL1	RW	0000_0000b	INT3 select enable register 1
0x28	PWM_IO_SEL	RW	xxxx_x000b	PWM select enable register
0x29	OSC_SFR_SEL	RW	xxxx_xx00b	Register ADJ_OSC valid value selection
0x2A	ADJ_OSC	RW	1111_1111b	Fine-tune the OSC system Clock register
0x2B	UART_IO_SEL	RW	xxxx_0000b	UART mapping I/O port select register
0x2C	IIC_IO_SEL	RW	xxxx_xx00b	IIC mapping IO port selection register
0x2D	ADC_CFG_SEL	RW	xxxx_xx00b	ADC control register
0x2E	BOR_LVDT_DEALY_SEL	RW	xxxx_x000b	BOR and LVDT delay selection register

Note:

1. **Registers whose addresses end in 8 or 0 can be operated by bit.**
2. **R: Only read; RW: Read and write.**
3. **'x': indeterminate state**
4. **'① ': The reset value is the default value after power-on reset, and the value after the global reset is completed is the factory calibration value.**

Steps to get the factory calibration value:

1. Turn off interrupt;
2. Configure the secondary bus address;
3. Read the data;
4. If you need to continue reading the data, go to steps 2 and 3;
5. Restore the interrupt setting.

4. Registers Summary

4.1. SFR Registers Details

DATAB (80H) PB data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB data register, configurable PB group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

SP (81H) Stack pointer register

Bit number	7	6	5	4	3	2	1	0
Symbol	SP[7:0]							
R/W	R/W							
Reset value	7							

DPL (82H) Data pointer register 0 low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	DPL[7:0]							
R/W	R/W							
Reset value	0							

DPH (83H) Data pointer register 0 high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	DPH[7:0]							
R/W	R/W							
Reset value	0							

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WAIT_MODE	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	WAIT_MODE	WAIT mode is enabled 1: The chip enters WAIT mode.

		0: The chip exits the WAIT mode
1~0	PLL_CLK_SEL	PLL clock divider selection register 00: 12MHz; 01: 6MHz; 10: 4MHz; 11: 1MHz

INT_PE_STAT (85H) WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status flag, this bit write 0 to clear zero, write WDT_CTRL operation can also clear 0 1: Interrupt is valid; 0: Interrupt is invalid
0	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is written 0 to clear, write TIMER2_CFG operation also can clear 0 1: Interrupt is valid; 0: Interrupt is invalid

INT_POBO_STAT (86H) LVDT power-on/brown-out interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	LVDT power-on interrupt status 1: Power-on interrupt is valid; 0: Power-on interrupt is invalid.
0	INT_BO_STAT	LVDT brown-out interrupt status. 1: Brown-out interrupt is valid; 0: Brown-out interrupt is invalid

PCON (87H) Low-power mode select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	LPM
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	LPM	Low-power mode control 1: Low-power mode; 0: Normal mode, automatically cleared after wake-up

TCON (88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
6	TR1	Timer1 start enable, when set to1, start Timer1, or start Time0 mode three, TH0 count.
5	TF0	Timer 0 overflow flag, set by hardware when Timer0 overflows.
4	TR0	Timer0 start enable, set to 1 to start Timer0 counting.
3	IE1	External interrupt 1 flag bit, set by hardware, cleared by software.
2	--	Reserved
1	IE0	External interrupt 0 flag bit, set by hardware, cleared by software.
0	--	Reserved

TMOD (89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer 1 mode select bit 00: Mode 0 - 13-bit timer 01: Mode 1 - 16-bit timer 10: Mode 2 - 8-bit timer with automatic reloading of initial value 11: Mode 3 - Two 8-bit timers
1~0	M0[1:0]	Timer 0 mode select bit 00: Mode 0 - 13-bit timer 01: Mode 1 - 16-bit timer 10: Mode 2 - 8-bit timer with automatic reloading of initial value 11: Mode 3 - Two 8-bit timers

TL0 (8AH) Timer 0 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TL1 (8BH) Timer 1 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH0 (8CH) Timer 0 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

TH1 (8DH) Timer 1 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

SOFT_RST (8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Soft reset register, only when the register value is 0x55, the software reset is generated

DATAC (90H) PC data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register, you can configure the output level when the IO port of the PC group is used as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

WDT_CTRL (91H) WDT timing overflow configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		

Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	WDT_TIME_SEL	WDT timing overflow configuration register, the timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

WDT_EN (92H) Watchdog timing enable configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	WDT_EN	Watchdog timing enable configuration register, when the configuration value is 0x55, the watchdog is closed

TIMER2_CFG (93H) TIMER2 configuration register

Bit number	7~3	2	1	0
Symbol	-	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	TIMER2_CLK_SEL	Timer2 clock selection register 1: Select XTAL 0: Select LIRC
1	TIMER2_RLD	TIMER2 auto reload enable register 1: Auto reload mode; 0: Manual reload mode
0	TIMER2_EN	TIMER2 count enable register Configure 1 to start timing, configure 0 to stop timing; In manual reload mode, the hardware will automatically clear this register after the count is completed, stop counting, and in automatic reload mode, the enable register will be maintained after the count is completed, and it will automatically restart; Counting from zero, no matter which mode, if this register is set to 1 during the counting process, it will start counting from zero.

TIMER2_SET_H (94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_H[7:0]	TIMER2 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER2_SET_L (95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_L[7:0]	TIMER2 count value configuration register, low 8 bits, the register will count again when configured during scanning.

REG_ADDR (96H) Secondary bus address configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-		REG_ADDR					
R/W	-		R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-		0	0	0	0	0	0

Bit number	Bit symbol	Description
7~6	-	Reserved
5~0	REG_ADDR	Secondary bus address configuration register: When operating the secondary bus register, it is recommended that RW secondary bus register first, EA = 0, then EA = 1. After the operation is completed, to prevent other interrupts or operations from modifying the secondary bus register address or data.

REG_DATA (97H) Secondary bus data read and write bus register

Bit number	7	6	5	4	3	2	1	0
Symbol	REG_DATA							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	REG_DATA	Secondary bus data read and write bus registeWhen RW secondary bus register is recommended, EA = 0 first, then EA = 1, after the operation is completed, to prevent other interrupts or operations from modifying the address or data of the secondary bus register.

DATAD (98H) PD data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD data register You can configure the output level of the PD group IO port as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

PWM1_L_L (99H) PWM1 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_L [7:0]							
R/W	R/W							
Reset value	0							

PWM1_L_H (9AH) PWM1 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_H [7:0]							
R/W	R/W							
Reset value	0							

PWM1_H_L (9BH) PWM1 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_L [7:0]							
R/W	R/W							
Reset value	0							

PWM1_H_H (9CH) PWM1 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H [7:0]							
R/W	R/W							
Reset value	0							

PWM2_L_L (9DH) PWM2 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_L [7:0]							

R/W	R/W
Reset value	0

PWM2_L_H (9EH) PWM2 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_H [7:0]							
R/W	R/W							
Reset value	0							

PWM2_H_L (9FH) PWM2 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_L [7:0]							
R/W	R/W							
Reset value	0							

P2_XH (A0H) MOVX @Ri, A operation pdata address high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	P2_XH [7:0]							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	P2_XH [7:0]	When using movx@ri, A instruction, P2_XH needs to clear 0 when operating pdata area.

PWM2_H_H (A1H) PWM2 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_H [7:0]							
R/W	R/W							
Reset value	0							

PWM_EN (A2H) PWM control register

Bit number	7	6	5	4
Symbol	-	-	PWM0_CH3_CMOD	PWM0_CH2_CMOD
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH1_CMOD	PWM2_EN	PWM1_EN	PWM0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5~3	PWM0_CHn_CMOD (n=3~1)	PWM0 channel n duty cycle mode select bit 1: Select PWM0_A (PWM0_A1) duty cycle;

		0: Select own channel duty cycle Channel 1: PWM0_B (PWM0_B1) Channel 2: PWM0_C (PWM0_C1) Channel 3: PWM0_D (PWM0_D1)
2	PWM2_EN	PWM2 module enable register 1: Enable; 0: Disable
1	PWM1_EN	PWM1 module enable register 1: Enable; 0: Disable
0	PWM0_EN	PWM0 module enable register 1: Enable; 0: Disable

PWM0_CH_CTRL (A3H) PWM0 control register

Bit number	7	6	5	4
Symbol	PWM0_CH3_POLA_SEL	PWM0_CH2_POLA_SEL	PWM0_CH1_POLA_SEL	PWM0_CH0_POLA_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH3_EN	PWM0_CH2_EN	PWM0_CH1_EN	PWM0_CH0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~4	PWM0_CHn_POLA_SEL (n=3~0)	Channel n polarity selection 1: The count value overflow makes the output low; 0: The count value overflow makes the output high; Channel 0: PWM0_A (PWM0_A1) Channel 1: PWM0_B (PWM0_B1) Channel 2: PWM0_C (PWM0_C1) Channel 3: PWM0_D (PWM0_D1)
3~0	PWM0_CHn_EN (n=3~0)	Channel n enable bit 1: Enable; 0: Disable

PWM0_CH0_CNT_L (A4H) PWM0 channel 0 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH0_CNT_L[7:0]	Channel 0 count value configuration register low 8

		bits Configure PWM output duty cycle

PWM0_CH0_CNT_H (A5H) PWM0 channel 0 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH0_CNT_H[7:0]	Channel 0 count value configuration register high 8 bits Configure PWM output duty cycle

PWM0_CH1_CNT_L (A6H) PWM0 channel 1 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH1_CNT_L[7:0]	Channel 1 count value configuration register low 8 bits Configure PWM output duty cycle

PWM0_CH1_CNT_H (A7H) PWM0 channel 1 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH1_CNT_H[7:0]	Channel 1 count value configuration register high 8 bits Configure PWM output duty cycle

IEN0 (A8H) Interrupt Enable Register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit

		0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer 1 overflow interrupt enable bit: 0: Disable timer 1 (TF1) to apply for interrupt; 1: Allow TF1 flag bit to request interrupt.
2	EX1	INT_EXT1 enable bit: 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 overflow interrupt enable bit: 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit: 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

PWM0_CH2_CNT_L (A9H) PWM0 channel 2 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH2_CNT_L[7:0]	Channel 2 count value configuration register low 8 bits Configure PWM output duty cycle

PWM0_CH2_CNT_H (AAH) PWM0 channel 2 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH2_CNT_H[7:0]	Channel 2 count value configuration register high 8 bits Configure PWM output duty cycle

PWM0_CH3_CNT_L (ABH) PWM0 channel 3 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0

Symbol	PWM0_CH3_CNT_L[7:0]
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	PWM0_CH3_CNT_L[7:0]	Channel 3 count value configuration register low 8 bits Configure PWM output duty cycle

PWM0_CH3_CNT_H (ACH) PWM0 channel 3 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH3_CNT_H[7:0]	Channel 3 count value configuration register high 8 bits Configure PWM output duty cycle

PWM0_MOD_L (ADH) PWM0 period configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_L[7:0]	PWM0 count period configuration register low 8 bits Configure the PWM output period

PWM0_MOD_H (AEH) PWM0 period configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_H[7:0]	PWM0 count period configuration register high 8 bits Configure the PWM output period

SCAN_START (AFH) LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W

Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LED scan open register 1: Scan start; 0: Scan close; In interrupt mode, the scan starts after the configuration is enabled. After that, the hardware is automatically cleared until the software configuration is enabled again. The software can also be directly configured and shut down In cyclic mode, the configuration remains unchanged after it is enabled until the software configuration is closed (the oftware ends immediately) and related signals inside the module are reset.

DP_CON (B0H) LED scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	DUTY_SEL			SCAN_MODE	COM_MOD
R/W	-	-	-	R/W			R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
4~2	DUTY_SEL	LED drive mode dot matrix selection configuration register 0: No matrix 1: 4x4 matrix(LED0~LED4); 2: 5x5 matrix(LED0~LED5); 3: 6x6 matrix(LED0~LED6); 4: 6x7 matrix(LED0~LED6); 5: 7x7 matrix(LED0~LED7); 6: 7x8 matrix(LED0~LED7); 7: 8x8 matrix(LED0~LED8)
1	SCAN_MODE	LED scan mode configuration 1: Cycle scan mode 0: Interrupt scan mode
0	COM_MOD	High current sink IO port drive enable 1: The COM locking function, as large current IO mouth work 0: The COM port is not locked and can be configured for other functions When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED scan configuration is invalid.

SCAN_WIDTH (B1H) LED scan on time 1 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	--	In LED dot matrix drive mode, corresponding to a single indicator time configuration register——Conduction time 1 set period=(scan_width+1)*16us, supports the configuration range0.016~4.096ms

LED2_WIDTH (B2H) LED scan on time 2 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In LED dot matrix drive mode, corresponding to a single indicator time configuration register——Conduction time 2 set period=(led2_width+1)*16us, supports the configuration range0.016~4.096ms

LED_DRIVE (B3H) LED driver capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
7~0	--	LED port drive capability configuration register 0~15—3.77mA~69.14mA, refer to the LED drive ammeter for details.

ADC_SPT (B4H) ADC sample time configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT	ADC sample time configuration register Sample time:Tsample = (ADC_SPT+1)*4*Tadc_clk

ADC_SCAN_CFG (B5H) ADC scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	ADC_ADDR					ADC_START
R/W	-	-	R/W					R/W
Reset value	-	-	0					0

Bit number	Bit symbol	Description
5~1	ADC_ADDR	ADC channel address selection register 000000: Corresponding to ADC0; 000001: Corresponding to ADC1; …… 11000: Corresponding to ADC24; 11001: Corresponding to ADC25; 11010: ADC26_VREF; Reserved all other values
0	ADC_START	ADC scan open register: 0: ADC module does not scan; 1: ADC module starts to scan ADC_START is set from 0 to 1, ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit. The ADC interrupt flag bit needs to be cleared by software. Note: ADC_START is not allowed to be configured during scanning

ADCCKC (B6H) ADC clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADCK	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
7~2	--	Reserved
1~0	ADCK	ADC_CLK frequency division selection 0: 3MHz 1: 2MHz 2: 1.5MHz 3: 1MHz

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1 (Timer1 interrupt) priority selection bit. 0: Low priority; 1: High priority
2	PX2	External interrupt 1 interrupt priority selection bit. 0: Low priority; 1: High priority
1	PT0	TF0 (Timer0 interrupt) priority selection bit. 0: Low priority; 1: High priority
0	PX0	External interrupt 0 interrupt priority selection bit. 0: Low priority; 1: High priority

ADC_RDATAH (B9H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RDATAH[3:0]			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	ADC_RDATAH[3:0]	ADC scan result register

ADC_RDATAL (BAH) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_RDATAL[7:0]	ADC scan result register

ADC_CFG1(BBH) ADC sample sequence control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADCWNUM					SAMBG	SAMDEL	
R/W	R/W					R/W	R/W	
Reset value	0					0	0	

Bit number	Bit symbol	Description
7~3	ADCWNUM	Selection of distance conversion interval time after sampling 00000: Reserved; 00001: Reserved; 00010: 5 ADC_CLK; 00011: 6 ADC_CLK; 00100: 7 ADC_CLK; ……

		11110: 33 ADC_CLK; 11111: 34 ADC_CLK;
2	SAMBG	Sample timing and comparison timing interval selection 0: Interval of 0 ADC_CLK; 1: Interval of 1 ADC_CLK
1~0	SAMDEL	Sample delay time selection 00: 0 ADC_CLK; 01: 2 ADC_CLK; 10: 4 ADC_CLK; 11: 8 ADC_CLK

ADC_CFG2 (BCH) ADC sample sequence control register 2

Bit number	7	6	5	4
Symbol	-	FILTER_R_SEL	VREF_IN_ADC_SEL	
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	ADC_I_SEL[1:0]		CTRL_SEL	-
R/W	R/W	R/W	R/W	-
Reset value	1	1	1	-

Bit number	Bit symbol	Description
6	FILTER_R_SEL	Input signal filter selection 0: No filtering; 1: Add 10K resistance filter, default value is 0
5~4	VREF_IN_ADC_SEL	Voltage selection for reference voltage input to ADC26_VREF 00: 1.433V; 01: 2.388V; 10: 3.306V; 11: 4.297V
3	ADC_I_SEL[1]	Operational amplifier bias current size selection signal 0 is 1 uA; 1 is 2uA. The default value is 1
2	ADC_I_SEL[0]	Comparator bias current size selection signal 0 is 1 uA; 1 is 2uA. The default value is 1
1	CTRL_SEL	Comparator maladjustment eliminates selection signals 0: Sample and then dissonance elimination; 1: All switches are turned off. The default value is 1
0	--	Reserved

UART0_BDL (BDH) UART0 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register Baud rate modulus divisor register, low 8 bits, Baud_Mod ={UART0_BDH[1:0], UART0_BDL}, When Baud_Mod = 0, no baud rate clock is generated, When Baud_Mod = 1~1023. Baud rate = BUSCLK/(16xBaud_Mod)

UART0_CON1 (BEH) UART0 control register1

Bit number	7	6	5	4
Symbol	-	UART0_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_ENABLE	Module enable, 1: Module enable, 0: Module disable
5	RECEIVE_ENABLE	Receiver enable, 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi-processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection, 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

UART0_CON2 (BFH) UART0 control register2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	-	-	R/W	R/W	R/W	
Reset value	-	-	-	-	1	1	0	0

Bit number	Bit symbol	Description
3	TX_EMPTY_IE	Transmit interrupt enable 1: Interrupt enable, 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable, 0: Interrupt disable (used in polling mode)
1~0	UART0_BDH	The upper 2 bits of the baud rate modulus divisor register

UART0_STATE (C0H) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/RW	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_R	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	The 9th data of the receiver, read only
5	UART0_T8	The 9th data of the transmittter, read only when parity check is enabled
4	TI0	Transmit interrupt flag: 1: Transmit buffer is empty 0: Transmit buffer is full, software write 0 to clear, write 1 is invalid
3	RI0	Receive interrupt flag: 1: Receive buffer is full 0: Receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	UART0_R	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	UART0_F	Frame error flag: 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	UART0_P	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

UART0_BUF (C1H) UART0 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Data register Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

UART_IO_CTRL (C2H) UART pin exchange control register

Bit number	7~2	1	0
Symbol	-	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	-	R/W	R/W
Reset value	-	0	0

Bit number	Bit symbol	Description
7~2	--	Reserved
1	UART1_PAD_CHANGE	UART1 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange
0	UART0_PAD_CHANGE	UART0 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange

UART_IO_CTRL1 (C3H) UART pin enable control register

Bit number	7~4	3	2	1	0
Symbol	-	UART1_RXD_DIASB	UART1_TXD_DIASB	UART0_RXD_DIASB	UART0_TXD_DIASB
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	UART1_RXD_DIASB	UART1 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
2	UART1_TXD_DIASB	UART1 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled
1	UART0_RXD_DIASB	UART0 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
0	UART0_TXD_DIASB	UART0 TXD port disable

		0: TXD pin is enabled; 1: TXD pin is disabled

LED_IO_START (C4H) LED start port control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	LED_IO_START[3:0]			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	LED_IO_START[3:0]	LED port matrix start PAD selection 0000: PB0; 0001: PB1; 0010: PB2; 0011: PB3; 0100: PB4; 0101: PB5; 0110: PB6; 0111: PB7; 1000: PC0 Others: PB0;

UART1_BDL (C5H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register Baud rate modulus divisor register, low 8 bits, Baud_Mod ={UART1_BDH[1:0], UART1_BDL}, When Baud_Mod = 0, no baud rate clock is generated, When Baud_Mod = 1~1023. Baud rate = BUSCLK/(16xBaud_Mod)

UART1_CON1 (C6H) UART1 control register1

Bit number	7	6	5	4
Symbol	-	UART1_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	--	Reserved
6	UART1_ENABLE	Module enable, 1: Module enable, 0: Module disable
5	RECEIVE_ENABLE	Receiver enable, 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi- processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection, 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

UART1_CON2 (C7H) UART1 control register2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	-	-	-	-	R/W	R/W	R/W	
Reset value	-	-	-	-	1	1	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	TX_EMPTY_IE	Transmit interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register, high 2 bits

UART1_STATE (C8H) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	R8	T8	TX_EMPTY_IF
R/W	-	R	R/RW	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	FRX_FULL_I	RX_OVERFLOW_IF	FRAME_ERR_IF	PARITY_ERR_IF
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	R8	The 9th data of the receiver, read only
5	T8	The 9th data of the transmitter, read only when parity check is enabled
4	TX_EMPTY_IF	Transmit interrupt flag: 1: Transmit buffer is empty 0: Transmit buffer is full, software write 0 to clear, write 1 is invalid
3	FRX_FULL_I	Receive interrupt flag: 1: Receive buffer is full 0: Receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	RX_OVERFLOW_IF	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	FRAME_ERR_IF	Frame error flag 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	PARITY_ERR_IF	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

UART1_BUF (C9H) UART1 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	-	UART1 data register Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

CSD_START (CAH) CSD scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	1: CSD scan is enabled; 0: CSD scan is stopped Write 1 to CSD_START to start the scan, after one scan is over, the hardware will automatically set it to 0. To start the next scan, the software needs to set it to 1 again; if CSD_START=0 during the scan, then the scan will stop immediately, and the relevant signals inside the module will be reset. Note: It must be used according to the process configuration: CSD_START=1, when an interrupt is detected, configure CSD_START=0. Configuration of CSD_START is not allowed during scan

SNS_SCAN_CFG1 (CBH) Touch key scan configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	SW_PRE_OFF	PRS_DIV					
R/W	-	R/W	R/W					
Reset value	-	0	0					

Bit number	Bit symbol	Description
6	SW_PRE_OFF	Front-end charge and discharge clock switch control. 1: Turn off sw_clk; 0: Turn on sw_clk
5~0	PRS_DIV	Front-end charge and discharge clock frequency selection register. 000000~ 111101: fixed frequency: F=F48M/2/(PRS_DIV+4)(6M~369K) 111110: The highest frequency is 3M, the lowest frequency is 1M, and the center frequency is 1.5M, normal distribution; 111111: The highest frequency is 3M, the lowest frequency is 1M, and the center frequency is 1.5M, uniform distribution

SNS_SCAN_CFG2 (CCH) Touch key scan configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	PULL_I_SELA_H	PARALLEL_EN	CSD_ADDR				
R/W	-	R/W	R/W	R/W				
Reset value	-	1	0	0				

Bit number	Bit symbol	Description
6	PULL_I_SELA_H	CSD pull-up current source configuration highest bit
5	PARALLEL_EN	SNS channel parallel enable register

		1: Multi -channel parallel; 0: Single channel
4~0	CSD_ADDR	Address of the detection channel, corresponding to the channel number 0~25 00000: SNS0; 00001: SNS1; 00010: SNS2; 00011: SNS3; 00100: SNS4; 00101: SNS5; 00110: SNS6; 00111: SNS7; 01000: SNS8; 01001: SNS9; 01010: SNS10; 01011: SNS11; 01100: SNS12; 01101: SNS13; 01110: SNS14; 01111: SNS15; 10000: SNS16; 10001: SNS17; 10010: SNS18; 10011: SNS19; 10100: SNS20; 10101: SNS21; 10110: SNS22; 10111: SNS23; 11000: SNS24; 11001: SNS25; Others: Reserved

SNS_SCAN_CFG3 (CDH) Touch key scan configuration register 3

Bit number	7	6	5	4
Symbol	-	RESO		
R/W	-	R/W		
Reset value	-	1	1	1
Bit number	3	2	1	0
Symbol	CSD_DS		PRE_CHRG_SEL	INIT_DISCHRG_SEL
R/W	R/W		R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~4	RESO	Counter bit selection register 000: 9 bits; 001: 10 bits; 010: 11 bits; 011: 12 bits; 100: 13 bits; 101: 14 bits; 110: 15 bits; 111: 16 bits
3~2	CSD_DS	Count clock frequency selection register 00: 24M; 01: 12M; 10: 6M; 11: 4M; default: 0
1	PRE_CHRG_SEL	Precharge time selection: 0: 20 μs; 1: 40μs
0	INIT_DISCHRG_SEL	Pre-discharge time selection: 0: 2μs; 1: 10μs

CSD_RAWDATAL (CEH) CSD count value low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAL[7:0]							
R/W	R							
Reset value	0							

CSD_RAWDATAH (CFH) CSD count value high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAH[7:0]							

R/W	R
Reset value	0

PSW (D0H) Program status word register

Bit number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS[1:0]		OV	F1	P
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	CY	Carry flag bit Set when addition generates carry or when subtraction generates debit, otherwise cleared. Set when the first operand of CJNE is less than the second operand, cleared by MUL and DIV directives. Also affected by mouse instructions (RLC, RRC) and bit-by-bit instructions.
6	AC	Auxiliary carry flag bit Set when the addition produces a carry from the accumulator's third to fourth digits, or when the subtraction produces a debit from the third to fourth digits, otherwise cleared.
5	F0	0 flag bit. Generic labels available to users.
4~3	RS[1:0]	Working register group selection: Select a valid working register group: RS[1:0] Bank IRAM Area 00 0 0x00-0x07; 01 1 0x08-0x0F; 10 2 0x10-0x17; 11 3 0x18-0x1F
2	OV	Overflow flag bit. When addition produces a different carry of accumulator bits 6 and 7, or subtraction produces a debit of accumulator bits 6 and 7. Otherwise clear. The OV flag bit indicates that the result of the signature's 8-digit number exceeds the limit (greater than 127 or less than -128). The overflow flag is also set when the multiplication result is greater than 255 or when an attempt is made to divide by 0.
1	F1	1 flag. Generic labels available to users.
0	P	Parity flag bit Always contains the sum of all bits of form 2 in the accumulator.

PULL_I_SELA_L (D1H) CSD pull-up current source selection register

Bit number	7	6	5	4	3	2	1	0

Symbol	PULL_I_SELA_L[7:0]
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	PULL_I_SELA_L[7:0]	CSD pull-up current source size selection switch; default is 0.

SNS_ANA_CFG (D2H) CSD scan parameter configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	RB_SEL			VTH_SEL		
R/W	-	-	R/W			R/W		
Reset value	-	-	1	0	1	1	1	1

Bit number	Bit symbol	Description
5~3	RB_SEL	RB resistor size selection 100: 60k; 101: 80k; Others: Reserved When used, Rb80k calibration value needs to be read from chip Information: CBYTE[0x404D]k/ 80K to calculate the normalized sensitivity proportioned
2~0	VTH_SEL	VTH voltage selection signal, 000: 1.5V; 001: 2.1V; 010: 2.5V, 011: 2.9V; 100: 3.2V; 101: 3.5V, 110: 3.9V; 111: 4.2V

SNS_IO_SEL1 (D3H) SNS channel selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL1[7:0]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 00000001 = SNS0; 00000010 = SNS1; 00000100 = SNS2; 00001000 = SNS3; 00010000 = SNS4; 00100000 = SNS5; 01000000 = SNS6; 10000000 = SNS7

SNS_IO_SEL2 (D4H) SNS channel selection register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL2 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL2[7:0]	SENSOR port selection enable bit\ 1: Select SENSOR; 0: Not select SENSOR 00000001 = SNS8; 00000010 = SNS9; 00000100 = SNS10; 00001000 = SNS11; 00010000 = SNS12; 00100000 = SNS13; 01000000 = SNS14; 10000000 = SNS15

SNS_IO_SEL3 (D5H) SNS channel selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL3 [23:16]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL3[23:16]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 00000001 = SNS16; 00000010 = SNS17; 00000100 = SNS18; 00001000 = SNS19; 00010000 = SNS20; 00100000 = SNS21; 01000000 = SNS22; 10000000 = SNS23

SNS_IO_SEL4 (D6H) SNS channel selection register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	SNS_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	SNS_IO_SEL4[1:0]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 01 = SNS24; 10 = SNS25

RST_STAT (D7H) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_F	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	1: BOOT address jump reset occurs. 0: Keep the original status
6	DEBUG_F	1: Modification configuration reset occurs; 0: Keep the original status
5	SOFT_F	1: Software reset occurs. 0: Keep the original status
4	PROG_F	1: Programming reset occurs; 0: Keep the original status
3	ADDROF_F	1: PC pointer overflows and resets. 0: Keep the original status
2	BO_F	1: Brown-out reset; 0: Keep the original status
1	PO_F	1: Power-on reset occurs. 0: Keep the original status
0	WDTRST_F	1: Watchdog timer overflow reset occurs; 0: Keep the original status

PD_PB (D8H) PB port pull-down resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD_PB7	PD_PB6	PD_PB5	PD_PB4	PD_PB3	PD_PB2	PD_PB1	PD_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PD_PBn (n=7~0)	PB port pull-down resistor enable register 1: Pull-down resistor enabled; 0: Pull-down resistor disabled;

ADC_IO_SEL1 (D9H) ADC select enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1[7:0]	Enable the ADC control function that disables analog

		input pins 1: Select ADC function; 0: Not select ADC function 00000001 = ADC00; 00000010 = ADC01; 00000100 = ADC02; 00001000 = ADC03; 00010000 = ADC04; 00100000 = ADC05; 01000000 = ADC06; 10000000 = ADC07

ADC_IO_SEL2 (DAH) ADC select enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2[7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001 = ADC08; 00000010 = ADC09; 00000100 = ADC10; 00001000 = ADC11; 00010000 = ADC12; 00100000 = ADC13; 01000000 = ADC14; 10000000 = ADC15

ADC_IO_SEL3 (DBH) ADC select enable register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3[7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001 = ADC16; 00000010 = ADC17; 00000100 = ADC18; 00001000 = ADC19; 00010000 = ADC20; 00100000 = ADC21; 01000000 = ADC22; 10000000 = ADC23

ADC_IO_SEL4 (DCH) ADC select enable register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_IO_SEL4[1:0]	

R/W	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
1~0	ADC_IO_SEL4[1:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 01 = ADC24; 10 = ADC25

PU_PA (DDH) PA port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PU_PA1	PU_PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	PU_PAn n=1~0	PA port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

PU_PB (DEH) PB port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PB7	PU_PB6	PU_PB5	PU_PB4	PU_PB3	PU_PB2	PU_PB1	PU_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PBn n=7~0	PB port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

PU_PC (DFH) PC port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PC7	PU_PC6	PU_PC5	PU_PC4	PU_PC3	PU_PC2	PU_PC1	PU_PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PCn n=7~0	PC port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

ACC (E0H) Accumulator

Bit number	7	6	5	4	3	2	1	0
Symbol	ACC							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ACC	Accumulator: The destination register is used for all arithmetic and logic operations.

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IE11	External Interrupt 3 interrupt flag 1: With interrupt flag 0: No interrupt flag
2	IE10	UART1 interrupt flag 1: With interrupt flag 0: No interrupt flag
1	IE9	UART0 interrupt flag 1: With interrupt flag 0: No interrupt flag
0	IE8	LVDT interrupt flag 1: With interrupt flag 0: No interrupt flag

PU_PD (E2H) PD port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PD7	PU_PD6	PU_PD5	PU_PD4	PU_PD3	PU_PD2	PU_PD1	PU_PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PDn n=7~0	PD port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

IICCON (E5H) IIC control register

Bit number	7	6	5	4
Symbol	-	-	IIC_RST	RD_SCL_EN
R/W	-	-	R/W	R/W
Reset value	-	-	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation, 0: IIC module works normally
4	RD_SCL_EN	The host reads the low clock line control bit 1: Enable the host to read and pull down the clock line function, 0: Disable the host read and pull down clock line function
3	WR_SCL_EN	The host writes the low clock line control bit, 1: Enable the function of writing and pulling down the clock line, 0: Disable the function of writing and pulling down the clock line
2	SCLEN	IIC clock enable bit: 1: Clock works normally, 0: Low the clock line
1	SR	IIC conversion rate control bit 1: The conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit: 1: IIC works normally, 0: IIC does not work

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-

R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
6	EX6	LED interrupt enable 1: Interrupt enable; 0: Interrupt disable;
5	EX5	Reserved
4	EX4	ADC interrupt enable 1: Interrupt enable; 0: Interrupt disable;
3	EX3	IIC interrupt enable 1: Interrupt enable; 0: Interrupt disable;
2	EX2	External Interrupt 2 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
1~0	-	Reserved

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	-	Reserved
3	EX11	External Interrupt 3 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
2	EX10	UART1 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
1	EX9	UART0 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
0	EX8	LVDT interrupt enable 1: Interrupt enable; 0: Interrupt disable;

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: Indicates that the start bit is detected; 0: Indicates that the start bit is not detected.
6	IIC_STOP	Stop signal flag 1: Means in the stop state; 0: Means that the stop bit is not detected.
5	IIC_RW	Read and write flag Record the read/write information obtained from the address byte after the last address match, 1: Indicates read operation; 0: Means write operation.
4	IIC_AD	Address data flag 1: Indicates that the most recently received or sent byte is data; 0: Indicates that the most recently received or sent byte is an address.
3	IIC_BF	IICBUF full flag bit: when receiving in IIC bus mode 1: Indicates that the reception is successful and the buffer is full; 0: Indicates that the reception is not completed and the buffer is still empty When transmitting in IIC bus mode: 1: Indicates that data transmission is in progress (not including the response bit and stop bit), and the buffer is still full; 0: Indicates that the data transmission has been completed (not including the response bit and stop bit), and the buffer is empty.
2	IIC_ACK	Reply flag

		1: Indicates an invalid response signal; 0: Indicates an effective response signal.
1	IIC_WCOL	Write conflict flag 1: Indicates that when the IIC is transmitting the current data, new data is trying to be written into the transmit buffer; the new data cannot be written into the buffer; 0: No write conflict occurred.
0	IIC_RECOV	Receive overflow flag 1: Indicates that new data is received when the previous data received by IIC has not been taken away, and the new data cannot be received by the buffer; 0: Indicates that no receive overflow has occurred.

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

TRISA (EAH) PA direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	Bit[1]~ Bit[1]: PA1~PA0 direction of port pins 0: PAx port is output; 1: PAx port is input

TRISB (EBH) PB direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PB7~PB0 port pins 0: PBx port is output; 1: PBx port is input

TRISC (ECH) PC direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PC7~PC0 port pins 0: PCx port is output; 1: PCx port is input

TRISD (EDH) PD direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PD7~PD0 port pins 0: PDx port is output; 1: PDx port is input

COM_IO_SEL (EEH) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, corresponding to PB port 1: Select COM port mode; 0: Select IO port mode

ODRAIN_EN (EFH) PA0/PA1/PD6 port open drain output enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2	--	PD6 open drain output enable register 1: Open drain output; 0: CMOS output
1	--	PA1 open drain output enable register 1: Open drain output;

		0: CMOS output
0	--	PA0 open drain output enable register 1: Open drain output; 0: CMOS output

B (F0H) B register

Bit number	7	6	5	4	3	2	1	0
Symbol	B							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	B	B register: the source and destination registers of multiplication and division operations.

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: With interrupt flag 0: No interrupt flag
6	IE6	LED interrupt flag 1: With interrupt flag 0: No interrupt flag
5	IE5	Reserved
4	IE4	ADC interrupt flag 1: With interrupt flag 0: No interrupt flag
3	IE3	IIC interrupt flag 1: With interrupt flag 0: No interrupt flag
2	IE2	External interrupt 2 interrupt flag 1: With interrupt flag 0: No interrupt flag
1~0	--	Reserved

PERIPH_IO_SEL (F2H) IIC/INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	-	-
R/W	-	R/W	R/W	-	-
Reset value	-	1	0	-	-
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		

Reset value	0	0	0	

Bit number	Bit symbol	Description
6	IIC_AFIL_SEL	IIC port analog filter selection enable 1: Select the analog filter function; 0: Not select the analog filter function
5	IIC_DFIL_SEL	IIC port digital filter selection enable 1: Select digital filter function; 0: Not select digital filter function
4~3	--	Reserved
2	INT2_IO_SEL	INT2 port selection enable 1: Select INT2 function; 0: Not select INT2 function
1	INT1_IO_SEL	INT1 port selection enable 1: Select INT1 function; 0: Not select INT1 function
0	INT0_IO_SEL	INT0 port selection enable 1: Select INT0 function; 0: Not select INT0 function

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IPL2.3	External Interrupt 3 interrupt priority 0: Low priority; 1: High priority
2	IPL2.2	UART1 interrupt priority 0: Low priority; 1: High priority
1	IPL2.1	UART0 interrupt priority 0: Low priority; 1: High priority
0	IPL2.0	LVDT interrupt priority 0: Low priority; 1: High priority

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority

		0: Low priority; 1: High priority
6	IPL1.6	LED priority 0: Low priority; 1: High priority
5	IPL1.5	CSD interrupt priority 0: Low priority; 1: High priority
4	IPL1.4	ADC interrupt priority 0: Low priority; 1: High priority
3	IPL1.3	IIC interrupt priority 0: Low priority; 1: High priority
2	IPL1.2	External interrupt 2 priority 0: Low priority; 1: High priority
1~0	--	Reserved

EXT_INT_CON (F7H) External interrupt polarity control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	INT3_ POLARITY	INT2_ POLARITY		INT1_ POLARITY		INT0_ POLARITY	
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	0	1	0	1	0	1

Bit number	Bit symbol	Description
6	INT3_POLARITY	External Interrupt 3 trigger polarity selection: 0: Falling edge (low-level wake-up in Sleep mode) 1: Rising edge (high level wake-up in Sleep mode)
5~4	INT2_POLARITY	External Interrupt 2 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
3~2	INT1_POLARITY	External Interrupt 1 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
1~0	INT0_POLARITY	External Interrupt 0 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)

DATAA (F8H) PA data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PA1	PA0
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA data register, you can configure the output level of the PA group IO port as GPIO port, the read value is the current level state of the IO port (input) or the configured output value (output)

SPROG_ADDR_H (F9H) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	**In non-BOOT upgrade mode:** Bit[7]: 0: Points to the DATA area address; 1: Reserved Bit[1:0]: The upper 2 bits of the address in the DATA area, { SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} indicates the DATA area address Bit[6:2]: Reserved **In BOOT upgrade mode:** Bit[6]: Reserved. Bit[7]: Select address to enable 0: Points to the DATA area address, {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]}; 1: Point to address 0x0000~0x3FFF, {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]}

SPROG_ADDR_L (FAH) Address register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	Indicates the low 8 bits of the address in the DATA area {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} represents the Address in the DATA area

SPROG_DATA (FBH) Data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	--	Data to be written

SPROG_CMD (FCH) Command configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x94: DATA area block erase; Write 0x95: DATA area sector erase; Write 0x96: DATA area page erase; Write 0x69: DATA area block word write; When data 0x12, 0x34, 0x56, 0x78, and 0x9A are continuously written, the BOOT upgrade mode is entered When data 0xfe, 0xDC, 0xBA, 0x98, and 0x76 are continuously written, the BOOT upgrade mode is exited If CFG_BOOT_EN=1 or the program is running in a non-boot space, the BOOT upgrade mode cannot be entered

SPROG_TIM (FDH) Erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	1	1	0	1	0

Bit number	Bit symbol	Description
7~5	SPROG_TIM[7:5]	Word write time configuration register 000: Word write time = 113.1μs, (word burn step 6 and 7) Others: Reserved;
4~0	SPROG_TIM[4:0]	The erase time is set to SPROG_TIM[4:0]=0~31 **In non-boot upgrade mode:** When SPROG_TIM[4:0] = 0~1, reserved When SPROG_TIM[4:0] = 2~25. DATA area erasure time = {1+2*SPROG_TIM[4:0]}+0.01 (ms) When SPROG_TIM[4:0] = 26~31. DATA area erasure time = 10.01 (ms) **When operating the main block in Boot upgrade mode:**

		When SPROG_TIM[4:0] = 0~25. CODE area erasure time = 20.01+5*SPROG_TIM[4:0] (ms) When SPROG_TIM[4:0] = 26~31. CODE area erasure time = 100.01 (ms)

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
7~5	--	Reserved
4	PD_LVDT	LVDT control register 1: Closed, 0: Open, closed by default
3	PD_BOR	BOR control register 1: Closed, 0: Open, open by default
2	PD_XTAL_32K	RTC crystal oscillator circuit (32768Hz/4MHz) control register 1: Closed, 0: Open, closed by default
1	PD_CSD	Simulate CSD work control register: 0: CSD module works normally; 1: CSD module does not work
0	PD_ADC	Analog ADC shutdown control register: 0: ADC module works normally; 1: ADC module does not work

BOR_LVDT_VTH (FFH) BOR and LVDT threshold select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	SEL_BOR_VTH[2:0]			SEL_LVDT_VTH[2:0]		
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
5~3	SEL_BOR_VTH[2:0]	BOR threshold select 010: 2.8V; 011: 3.3V; 100: 3.7V; 101/110/111: 4.2V 000/001: Reserved After power-on reset, the default BOR threshold is

		2.1V, the program configures the above gear.
2~0	SEL_LVDT_VTH[2:0]	LVDT threshold select 000: Reserved; 001: 2.7V; 010: 3.0V; 011: 3.3V; 100: 3.6V; 101: 3.9V; 11x: 4.2V

Note:"-" indicates Reserved, Reserved register, and Reserved bit of register. Write operations are prohibited; otherwise, chip exceptions may occur.

4.2. Secondary Bus Registers Details

CFG0_REG (00H) Configuration word register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG1_REG (01H) Configuration word register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	01							

CFG2_REG (02H) Configuration word register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	1D							

CFG3_REG (03H) Configuration word register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	3F							

CFG4_REG (04H) Configuration word register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	C9							

CFG5_REG (05H) Configuration word register 5

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	CD							

CFG6_REG (06H) Configuration word register 6

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG7_REG (07H) Configuration word register 7

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	3F							

CFG8_REG (08H) Configuration word register 8

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	64							

CFG9_REG (09H) Configuration word register 9

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	7F							

CFG10_REG (0AH) Configuration word register 10

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0F							

CFG11_REG (0BH) Configuration word register 11

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG12_REG (0CH) Configuration word register 12

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	07							

CFG13_REG (0DH) Configuration word register 13

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	03							

CFG14_REG (0EH) Configuration word register 14

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG15_REG (0FH) Configuration word register 15

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG16_REG (10H) Configuration word register 16

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG17_REG (11H) Configuration word register 17

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	03							

CFG18_REG (12H) Configuration word register 18

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG19_REG (13H) Configuration word register 19

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG20_REG (14H) Configuration word register 20

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG21_REG (15H) Configuration word register 21

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							

Reset value	2A

CFG22_REG (16H) Configuration word register 22

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	01							

CFG31_REG (17H) Configuration word register 31

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	07							

CFG30_REG (1AH) Configuration word register 30

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

XTAL_CLK_SEL (20H) Crystal clock selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	XTAL_CLK_SEL
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	XTAL_CLK_SEL	RTC crystal circuit selection register 1: XTAL4MHz; 0: XTAL32768Hz

BOOT_CMD (21H) Program space jump instruction register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_CMD[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	BOOT_CMD[7:0]	Configure the program space jump instruction, Write 5 consecutive groups of data into the main program space: 0xff, 0x00, 0x88, 0x55, 0xaa Write five groups of data to boot: 0x37, 0xc8, 0x42, 0x9a, 0x65 The value read out is the byte written recently

ROM_OFFSET_L (22H) Address offset of the CODE field low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	The address offset of the CODE field(low 8 bits)

ROM_OFFSET_H (23H) Address offset of the CODE field high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	The address offset of the CODE field(high 8 bits)

BOOT_EN (24H) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	BOOT_EN
R/W	-	-	-	-	-	-	-	R
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	BOOT_EN	1: Indicates that the BOOT upgrade mode has been entered, 0: Indicates that the BOOT upgrade mode has been exited. Note: In BOOT upgrade mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as BOOT upgrade function.

PERIPH_IO_SEL3 (25H) INT3 select enable register 3

Bit number	7	6	5	4
Symbol	-	INT3_22_IO_SEL	INT3_21_IO_SEL	INT3_20_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	INT3_19_IO_SEL	INT3_18_IO_SEL	INT3_17_IO_SEL	INT3_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description

6~0	INT3_n_IO_SEL (n=22~16)	INT3_n port selection enable 1: Select INT function 0: Not select INT function

PERIPH_IO_SEL2 (26H) INT3 select enable register 2

Bit number	7	6	5	4
Symbol	INT3_15_IO_SEL	INT3_14_IO_SEL	INT3_13_IO_SEL	INT3_12_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_11_IO_SEL	INT3_10_IO_SEL	INT3_9_IO_SEL	INT3_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=15~8)	INT3_n port selection enable 1: Select INT function 0: Not select INT function

PERIPH_IO_SEL1 (27H) INT3 select enable register 1

Bit number	7	6	5	4
Symbol	INT3_7_IO_SEL	INT3_6_IO_SEL	INT3_5_IO_SEL	INT3_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_3_IO_SEL	INT3_IO_2_SEL	INT3_1_IO_SEL	INT3_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=7~0)	INT3_n port selection enable 1: Select INT function 0: Not select INT function

PWM_IO_SEL (28H) PWM select enable register

Bit number	7~3	2	1	0
Symbol	-	PWM2_IO_SEL	PWM1_IO_SEL	PWM0_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved

2	PWM2_IO_SEL	PWM2 port selection enable 0: PD1 port selects PWM2_A function 1: PC7 port selects PWM2_A1 function
1	PWM1_IO_SEL	PWM1 port selection enable 0: PD0 port selects PWM1_A function 1: PC6 port selects PWM1_A1 function
0	PWM0_IO_SEL	PWM0 port selection enable 0: PB0/1/2/3 port select PWM0_A/B/C/D function 1: PB5/PC0/PC3/PC5 port select PWM0_A1/B1/C1/D1 function

OSC_SFR_SEL (29H) Register ADJ_OSC valid value selection

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	--	Register ADJ_OSC valid value selection 10: Select SFR write value; Others: Select the configuration word 6 Note: read the OSC calibration value and control it within ±10% of the calibration value of CFG6_REG[7:0]

ADJ_OSC (2AH) Fine-tune the OSC system clock register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADJ_OSC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Configuration word register,Fine-tune the OSC system clock The write value is SFR, the read value is valid, and it selects the configuration word 6 or SFR based on OSC_SFR_SEL

UART_IO_SEL (2BH) UART mapping IO port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	UART1_IO_SEL	UART0_IO_SEL		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	UART1_IO_SEL	UART1 port selection enable

		0: PB1/2(RXD1_A/TXD1_A) port select UART1 function 1: PB6/7(RXD1_B/TXD1_B) port select UART1 function
2~0	UART0_IO_SEL	UART0 port selection enable 000: PA0/1(RXD0_A/TXD0_A) port select UART0 function 001: PB3/4(RXD0_B/TXD0_B) port select UART0 function 01x: PC0/1(RXD0_D/TXD0_D) port select UART0 function 100: PD6/PA1(RXD0_E/TXD0_E) port select UART0 function 101: PD7/PA0(RXD0_F/TXD0_F) port select UART0 function 11x: PD4/5(RXD0_C/TXD0_C) port select UART0 function

IIC_IO_SEL (2CH) IIC mapping IO port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	IIC_IO_SEL	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	IIC_IO_SEL	IIC port selection enable 00: PA0/PA1 port select IIC function 01: PB5/PC0 port select IIC function 10: PA1/PD6 port select IIC function 11: Reserved When PB5/PC0 serves as an IIC port, there is no SR control function, and the automatic logic control changes to open leakage output. When PB5/PC0 serves as GPIO, there is no open leakage output function

ADC_CFG_SEL (2DH) ADC control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_VREF_SEL	ADC_VREF_VOL_SEL
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	ADC_VREF_VOL_SEL	ADC_VREF output mode selection signal. 0: 2 V is used as ADC reference voltage 1: 4V is used as an ADC reference voltage
0	ADC_VREF_SEL	Select the source of the output signal. 0: Select VCC as the output signal 1: Select the output of ADC_VREF module as the

		output signal

BOR_LVDT_DEALY_SEL (2EH) BOR and LVDT delay selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	BOR_DELAY_SEL	LVDT_DELAY_SEL	
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2	BOR_DELAY_SEL	BOR delay selection 0: Delay selection 1; 1: Delay selection 2
1~0	LVDT_DELAY_SEL	LVDT delay selection 0: Delay time 1; 1: Delay time 2; 2: Delay time 3; 3: Delay time 4

Note: "-" indicates reservation. Reserved registers and reserved bits of registers. Write operations are prohibited. Otherwise, chip exceptions may occur.

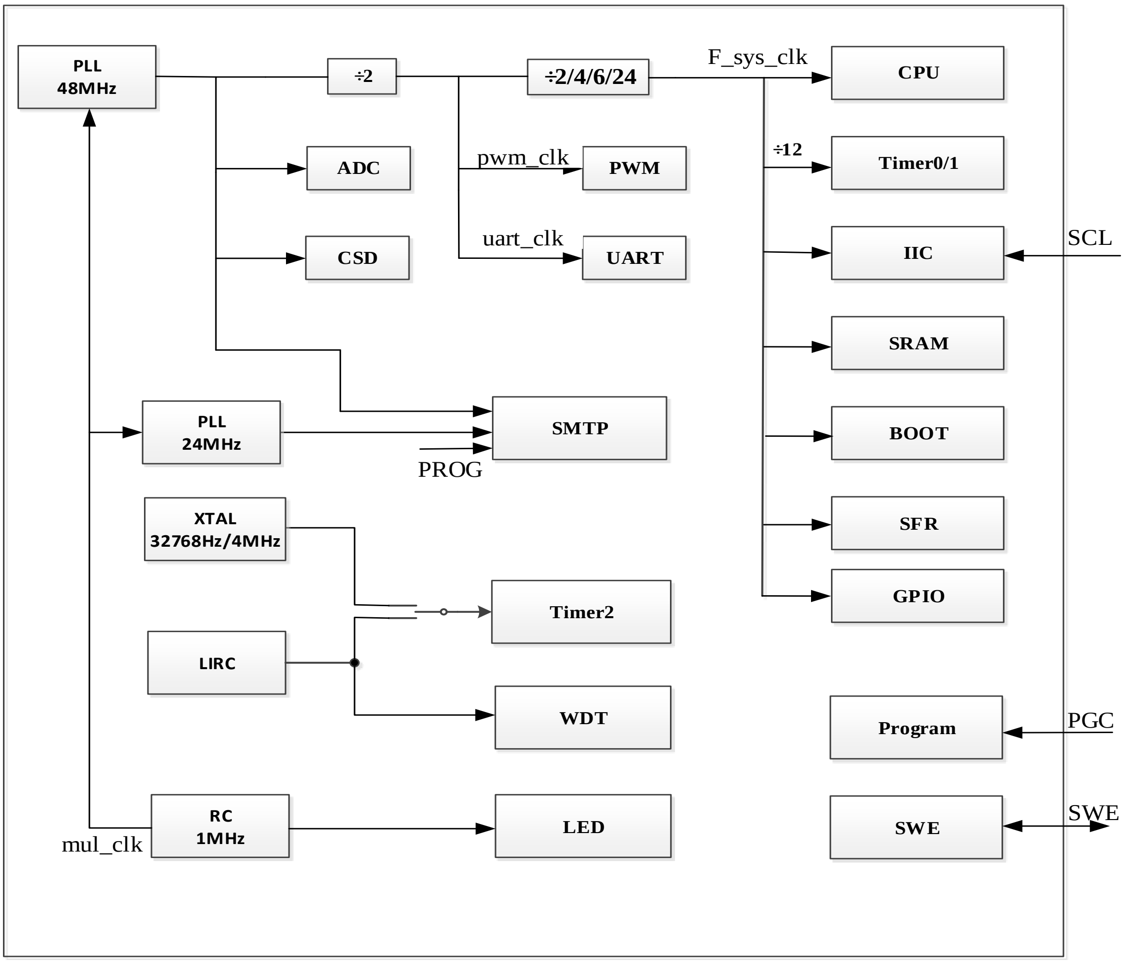
5. Clock, Reset, Working Mode and Watchdog

5.1. Clock

5.1.1 Clock definition

Clock source:

- Internal high-speed RC oscillator: RC1M
- Internal low-speed RC oscillator: LIRC32k
- External crystal oscillator: 32768 Hz/4 MHz
- The PLL clock is obtained by multiplying the frequency of RC1M: PLL48M/ PLL24M



Clock block diagram

The BF7612DMXX-SJLX series clocks are used in the following Modules:

RC1MHz: Built-in RC oscillator, the frequency is 1MHz, this clock is used as LCD/LED Driver clock.

mul_clk: Multiply RC1M to get the PLL clock;

PLL_48MHz: The 48MHz clock generated by the phase-locked loop is used as the clock source of

ADC
F_sys_clk: 12 MHz/6 MHz/4 MHz/1 MHz, can be used as core related clock;
pwm_clk: 24MHz, PWM clock;
uart_clk: 24MHz, UART clock;
PLL_24MHz: The 24MHz clock generated by the phase-locked loop is used as the main system clock after frequency division.
XTAL32768Hz/4MHz: External crystal clock 32768Hz/4MHz, can be used as Timer2 clock;
LIRC: Internal low-speed clock 32768Hz, which is used as watchdog clock and Timer2 clock; internal low-speed clock 32768Hz, which is used as watchdog clock and Timer2 clock;
SCL: The frequency is 100 kHz/400 kHz, as the IIC communication clock.
PGC: Programming clock, frequency range of 100 kHz~5MHz, programming burning program download clock.

5.1.2. Clock Registers

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WAIT_MODE	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
1~0	PLL_CLK_SEL	PLL clock divider selection register 00: 12MHz; 01: 6MHz; 10: 4MHz; 11: 1MHz

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
2	PD_XTAL_32K	RTC crystal resonance circuit (32768Hz/4MHz) control register 1: Closed, 0: Open, closed by default

Secondary bus register

XTAL_CLK_SEL (20H) Crystal clock selection register

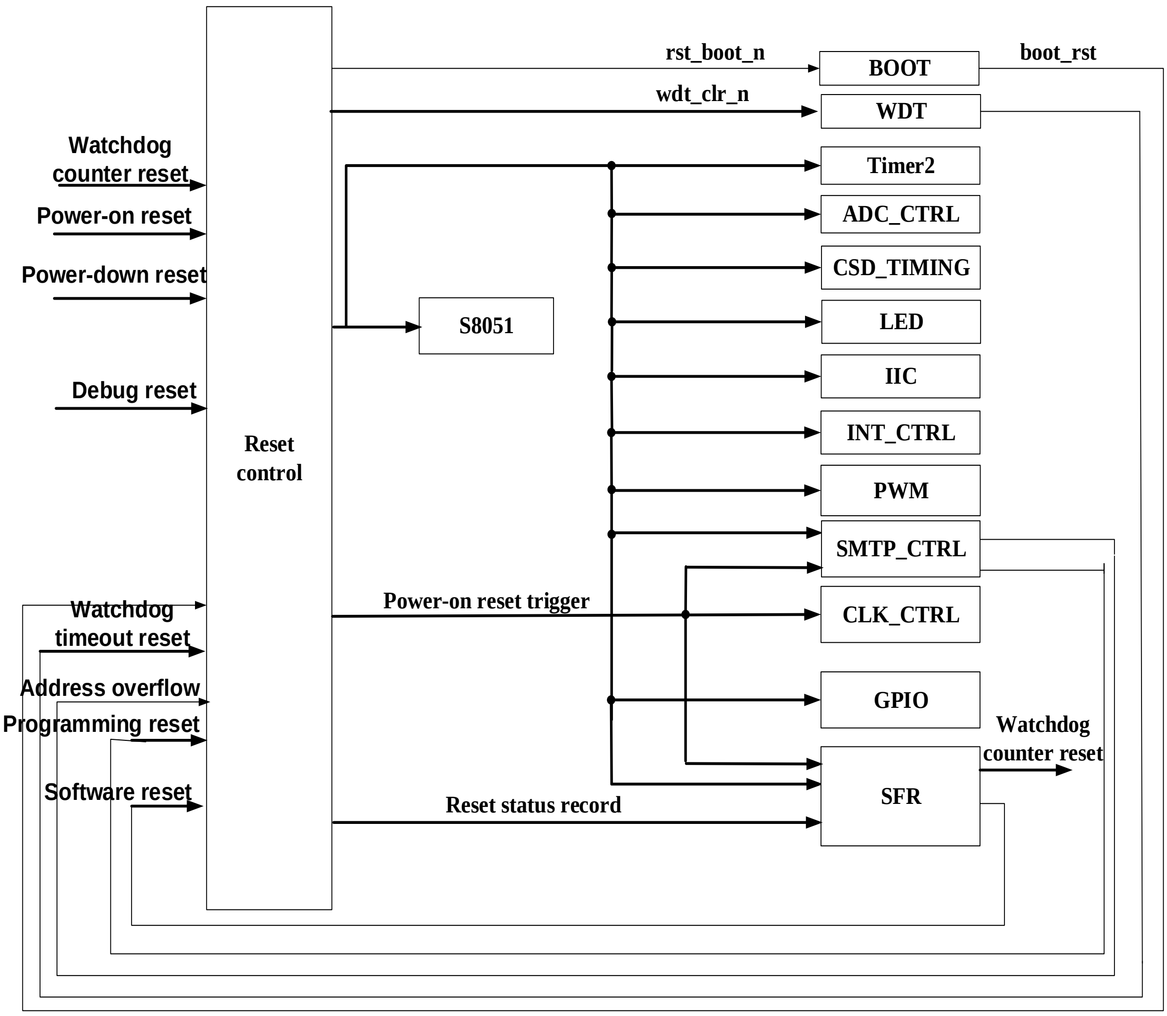
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	XTAL_CLK_SEL

R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	XTAL_CLK_SEL	RTC crystal circuit selection register 1: XTAL4MHz; 0: XTAL32768Hz

5.2. Reset System

There are 8 reset modes in the BF7612DMXX-SJLX: WDT overflow reset, power on reset (POR), brown-out reset (BOR), programming reset, modified configuration reset, PC pointer overflow reset, software reset, BOOT address jump reset. Any one of above reset, global will make chip reset. We can judge the reset flag register which reset happen, the reset must be cleared by software.



Reset block diagram

5.2.1. Reset Sequence

po_n: power-on reset. After the system is powered on, the analog module generates a low-level signal and lasts for 155ms. When the power-on reset is low, the entire chip is in the reset state, and after the global reset signal continues to be effective 40ms after the power-on reset is high, the system exits the reset mode.

bo_n: brown-out reset. The analog module generates a low-level signal after the system has a power-down reset. When the power-down reset signal is low, the entire chip is in the reset state. After the global reset signal becomes high, the system exits the reset mode after the global reset signal continues to be valid for 20ms.

soft_rst: software reset. The soft reset signal is valid by writing SFR, and the global reset signal is valid for 20ms. After 20ms, the system exits the reset mode.

prog_en: programming reset. When prog_en is high, it is the programming mode of SMTP. At this time, the global reset signal is valid. After it goes low, the global reset signal continues to be valid for 20ms.

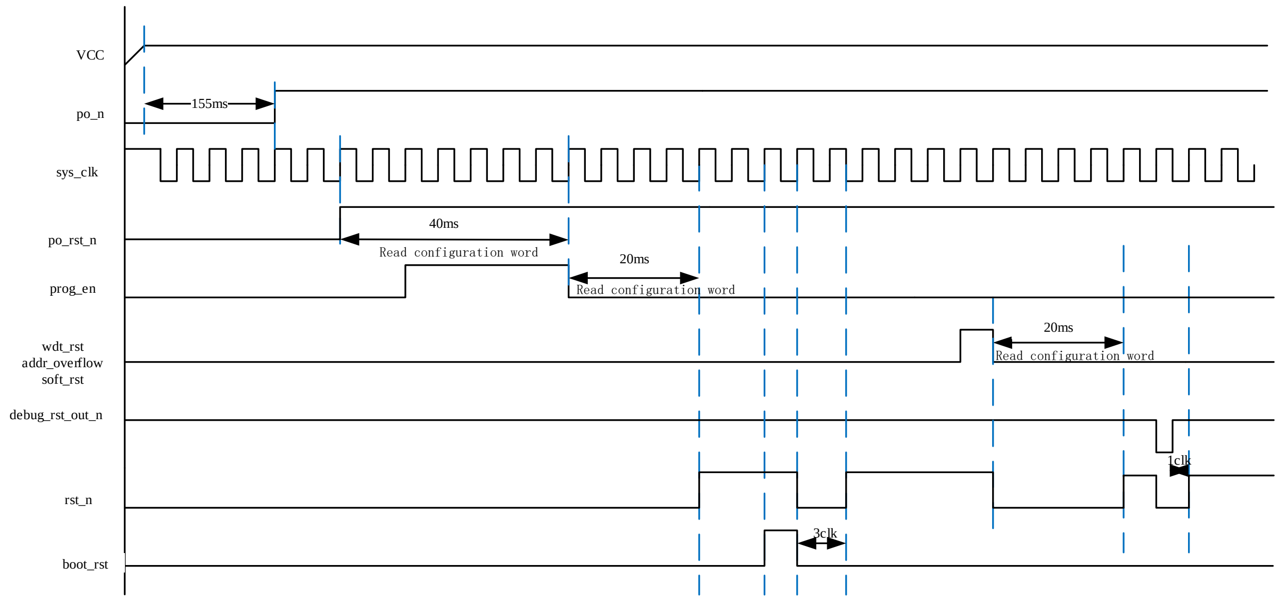
wdt_rst: The watchdog timer overflows and resets. After the watchdog timer overflows, the global reset is 20ms. After 20ms, the system exits the reset mode.

addr_overflow: PC pointer overflow reset. If the PC pointer exceeds the valid address range of the SMTP when the MCU addresses the program memory, the addr_overflow signal becomes high, and the sys_clk clock rising edge detects the high level of addr_overflow (requires 1 clock cycle) and resets the global 20ms, the reset signal will clear the addr_overflow signal to zero. After 20ms, the system exits the reset mode.

debug_rst_out_n: Trim configuration reset, output a reset signal for the core trim module, low means reset is effective, chip global reset, but there will not be a 20ms initialization process, only delay 1 system clock reset low level.

boot_rst: ROM address jump reset, the boot_rst signal becomes high after the complete ROM space jump instruction is configured, and the sys_clk clock checks the boot_rst high level (valid for one clock cycle) to reset the global, but there will be no 20ms read configuration word process. Only delay the reset low level of 3 System clocks.

Reset sequence description:

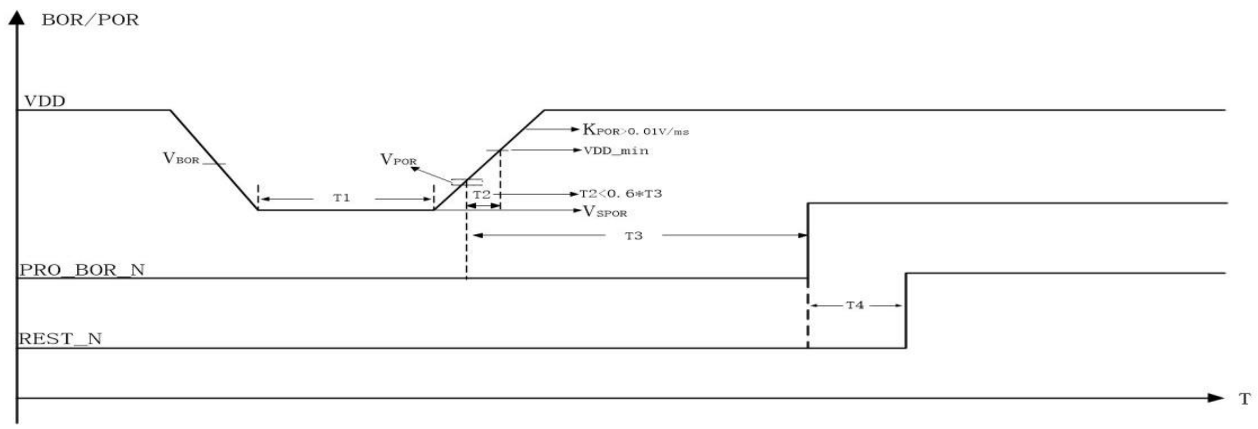


1. The chip has a power-on reset, and the analog POR module delays for 93ms, and po_n is pulled high.
2. The programmer sends instructions to make the chip enter the programming mode (prog_en is pulled high). In the programming mode, the system is in a global reset state. After the programming is completed, the programming mode is exited. After a delay of 20ms, rst_n is pulled high and the chip enters normal operation.
3. During normal operation, any one of watchdog reset, address overflow reset, soft reset, ROM address jump reset occurs, rst_n is pulled low, after a delay of 20ms, rst_n is pulled high, and the chip enters normal operation.
4. After normal work, you cannot enter the programming mode.
5. In debug mode, configure debug reset, pull down rst_n, pull up 1 system clock in

debug_rst_out_n, pull up rst_n, and the chip enters normal operation.

6. When the chip supports the BOOT upgrade function, a ROM Address jump reset occurs, rst_n is pulled low, after 3 System clocks, rst_n is pulled high, and the chip enters normal operation.

BO / PO chart:



BOR/POR chart diagram

BOR/POR parameter:

Symbol	Parameter	Min	Typ	Max	Unit
VSPOR	Power on reset start voltage	-	-	300	mV
KPRO	Power on reset voltage rate	0.01	-	5	V/ms
VPOR	Power on reset voltage	1.1	1.5	2.2	V
VBOR	Brown-out reset voltage (±10%), hysteresis 0.2V	-	VBOR	-	V
VDD_min	Minimum operating voltage	2.7	-	-	V
T1	VDD keep VSPOR time	0.1	-	-	ms
T2	VPOR from VDD_min time	-	-	0.6*T3	ms
T3	Reset POR_BOR_N duration	92	155	218	ms
T4	Global reset effective time	-	40	-	ms

Power on reset parameter characteristic table

Note:

1. **The power-on reset voltage rate KPRO is recommended to be less than 5 V/ms (that is, the power-on time of 0~5V is recommended to be greater than 1ms).**
2. **The VBOR power-down reset voltage is selected by register SEL_BOR_VTH[2:0].**
3. **When VDD is affected by the load or seriously interfered, if the voltage drops into the voltage dead zone and the chip is not within the working voltage range, it may cause abnormal system operation, such as data loss in the DATA area. The function of power-down reset (BOR) is to monitor that when VDD drops to the BOR voltage, the MCU can generate a power-down reset in advance to avoid system errors. Suggestion to prevent entering the voltage dead zone and reduce the probability of system error: increase the voltage drop slope.**

5.2.2. Reset Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0xD7	RST_STAT	RW	0000_0010b	Reset flag register
0xFE	PD_ANA	RW	xxx1_0111b	Module switch control register
0xFF	BOR_LVDT_VTH	RW	xx00_0000b	BOR and LVDT threshold select register

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x2E	BOR_LVDT_DEALY_SEL	RW	xxxx_x000	BOR and LVDT delay selection register

RST_STAT (D7H) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_F	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	1: BOOT address jump reset occurs. 0: Keep the original status
6	DEBUG_F	1: Modification configuration reset occurs; 0: Keep the original status
5	SOFT_F	1: Software reset occurs. 0: Keep the original status
4	PROG_F	1: Programming reset occurs; 0: Keep the original status
3	ADDROF_F	1: PC pointer overflows and resets. 0: Keep the original status
2	BO_F	1: Brown-out reset; 0: Keep the original status
1	PO_F	1: Power-on reset occurs. 0: Keep the original status
0	WDTRST_F	1: Watchdog timer overflow reset occurs; 0: Keep the original status

SOFT_RST (8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							

R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	--	Soft reset register, only when the register value is 0x55. the software reset is generated

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
3	PD_BOR	BOR control register 1: Closed, 0: Open, open by default

BOR_LVDT_VTH (FFH) BOR and LVDT threshold select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	SEL_BOR_VTH[2:0]			SEL_LVDT_VTH[2:0]		
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
3	SEL_BOR_VTH[2:0]	BOR threshold select 010: 2.8V; 011: 3.3V; 100: 3.7V; 101/110/111: 4.2V 000/001: Reserved After power-on reset, the default BOR threshold is 2.1V, the program configures the above gear.

Secondary bus registers

BOR_LVDT_DEALY_SEL (2EH) BOR and LVDT delay selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	BOR_DELAY_SEL	LVDT_DELAY_SEL	
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2	BOR_DELAY_SEL	BOR delay selection 0: Delay selection 1; 1: Delay selection 2

BOR: power supply voltage 5V→0.5V→5V, time interval 100ms, T=25℃					
Delay selection	threshold select <2:0>	Brown-out threshold (V)	Restore threshold (V)	Hysteresis voltage (mV)	Delay time (us)
Delay selection 1	010	2.8	2.9	136.2	105.2
	011	3.3	3.5	143.4	138.3
	100	3.7	3.8	120.5	163
	101/110/111	4.2	4.3	128.8	193.7
Delay selection 2	010	2.8	2.9	141	210.4
	011	3.3	3.5	149.6	277.1
	100	3.7	3.8	127.9	327
	101/110/111	4.2	4.3	137.5	389

5.3. Work Mode

5.3.1. Overview

The BF7612DMXX-SJLX series has 3 working modes, which can be selected according to different situations.

The BF7612DMXX-SJLX provides SYS_CLK_CFG register, whose Bit2 can be configured to control MCU into Wait mode. The BF7612DMXX-SJLX provides PCON register, whose Bit0 can be configured to control MCU into low power mode.

- **Normal mode**

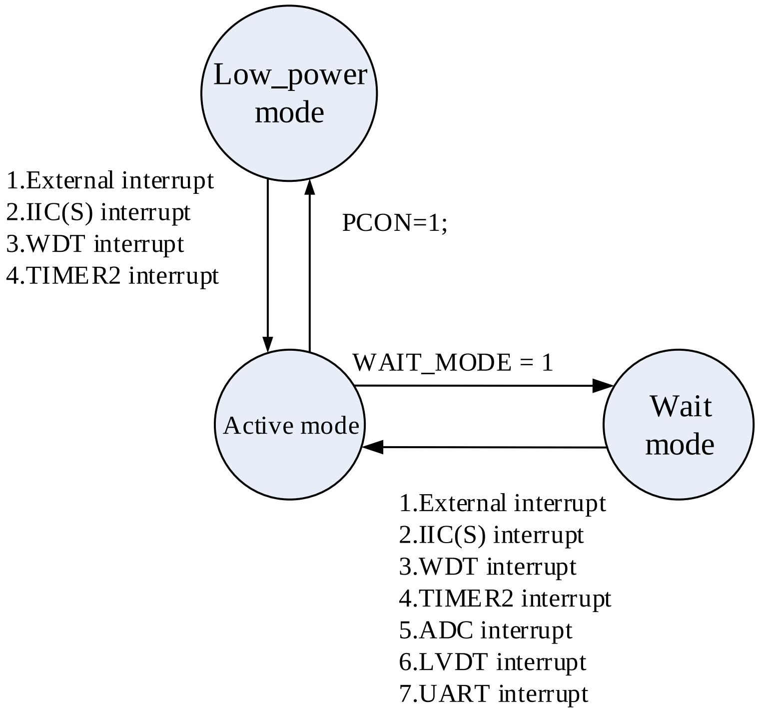
That is, in normal working mode, the module keeps working normally, and the functions of each module are controlled by software configuration.

- **Wait mode**

Write 1 to SYS_CLK_CFG.2 to enter the Wait mode. Core related modules and uart0~1. SPI, pwm0~2 modules do not work, the other modules can all work and exit this mode through interrupts.

- **Low power mode**

Write 1 to PCON.0 to enter low power consumption mode. At this time, RC1M and PLL are closed, LIRC works, WDT/TIMER2 can be configured to work, CPU and other digital modules do not work



Working mode conversion diagram

In addition, all modules can be individually configured to close the gate to reduce power consumption. For example, in normal mode, you can configure to turn off the CPU and system module clocks, and only enable modules such as LED/CSD/ADC to work;

Ways to exit the Wait mode:

- Enabling any one of IIC, External Interrupt 0, External Interrupt 1, External Interrupt 2, External Interrupt 3, WDT, Timer2, LED, CSD, ADC, LVDT to wake up the chip; Exit the Wait mode, and the CPU executes the interrupt service routine.

Ways to exit Low_power mode:

- Enabling IIC, External Interrupt 0, External Interrupt 1, External Interrupt 2, External Interrupt 3, WDT, Timer2 interrupt generation can wake up the chip; Exit Low_power mode, after the interrupt response is generated. The CPU executes the interrupt service program related to the interrupt vector, and returns to the next instruction after the execution of the RETI return instruction to make the CPU enter the Low_power mode to continue running the program.

Note: PCON = 0x01, lower power consumption can be obtained by turning off BOR, but the chip needs to be in the normal operating voltage range (2.7V~5.5V). If the chip power supply is unstable and lower than 2.7V, it is strongly recommended to turn on BOR.

Mode	Conditions for entering the mode	Effect on the clock	
Active/Wait	PCON=0	LIRC	Work
		XTAL32K	Depends on software configuration
		RC1M	Work
		PLL	Work
Low Power	PCON=1	LIRC	Work
		XTAL32K	Depends on software configuration
		RC1M	Close
		PLL	Close

The working state table of the clock source in each mode

NO	Module	Clock source	Working status		
			Active	Wait	Low Power
1	s8051	PLL_48M	√	×	×
2	UART0/1	PLL_48M	According configuration	×	×
3	PWM	PLL_48M	According configuration	×	×
4	Internal Timer0	PLL_48M	According configuration	×	×
5	Internal Timer1	PLL_48M	According configuration	×	×

6	External Timer2	LIRC/ XTAL32K /4MHz	According configuration	According configuration	According configuration
7	LED	RC1M	According configuration	According configuration	×
8	WDT	LIRC	According configuration	According configuration	According configuration
9	ADC_CTRL	PLL_48M	According configuration	According configuration	×
10	CSD_Timing	PLL_48M	According configuration	According configuration	×
11	IIC(S)	PLL_48M	According configuration	According configuration	According configuration

Status table of each digital module in different modes

5.3.2. Registers

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WAIT_MODE	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	WAIT_MODE	The WAIT mode is enabled 1: The chip enters WAIT mode. 0: the chip exits the WAIT mode

PCON (87H) Low-power mode select register

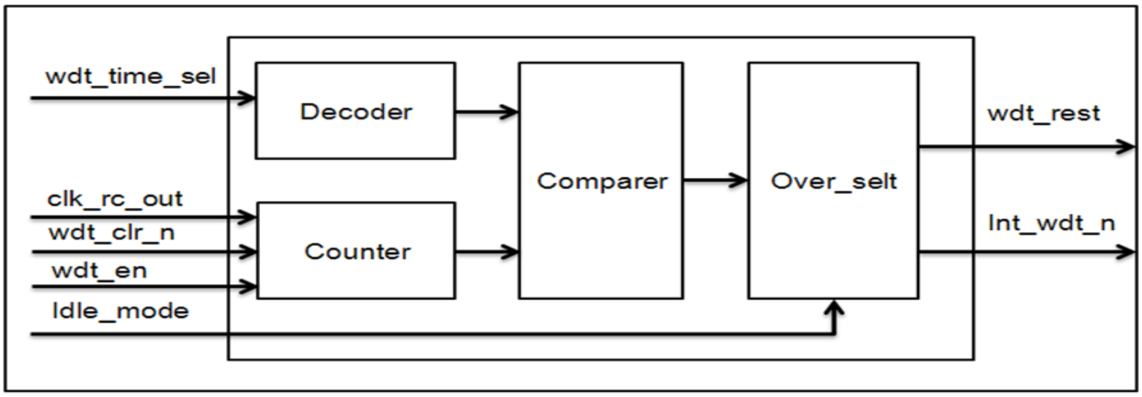
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	LPM
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	LPM	Low-power mode control 1: Low-power mode; 0: Normal mode, automatically cleared after wake-up

5.4. WDT

5.4.1. WDT Function Description

The watchdog timer counting circuit uses the internal low-speed clock LIRC for timing, and the configurable timing time is 2^n*18ms (n=0, 1. 2. 3. 4. 5. 6, 7) ----- here n is the configuration value of the timing configuration register.



Due to the particularity of the system application, the watchdog timer overflow signal is classified:

In the normal working mode, if the watchdog timer overflow occurs, the overflow signal is the watchdog overflow reset signal at this time, and the watchdog overflow reset affects the global reset. At this time, the system realizes the global reset action and reloads the configuration information;

In the low-power mode, if a watchdog timer overflow occurs, the overflow signal is the watchdog interrupt signal at this time, and the interrupt wakes up the chip to exit the low-power mode and execute the watchdog interrupt service function.

The watchdog module is a timing counting module. Its count clock is the internal low-speed clock LIRC. Its timing clear signal is composed of global reset and configuration clear. This signal is synchronously released by the watchdog timing clock in the reset module; The clearing action is generated every time the CPU configures the watchdog timer configuration register (WDT_CTRL), and the watchdog restarts timing; at the same time, the watchdog counter has the watchdog count enable control, when the count enable is valid, After the watchdog generates a timing overflow (reset or interrupt), as long as the watchdog counting enable is not turned off, the watchdog counter will restart counting

Write 0x55 to turn off the watchdog. Write other values to turn on the watchdog. The watchdog timer works after the reset. Watchdog timer zeroing is done by writing the WDT_CTRL register, and whatever value is written into the register will cause the watchdog timer to zeroing.

5.5.2. Registers

SFR register				
Address	Name	RW	Reset value	Description
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow configuration register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1

INT_PE_STAT (85H) WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status flag, this bit write 0 to clear zero, write WDT_CTRL operation can also clear 0 1: Interrupt is valid; 0: Interrupt is invalid;

WDT_CTRL (91H) WDT timing overflow configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	WDT_TIME_SEL	WDT timing overflow configuration register, the timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

WDT_EN (92H) Watchdog timing enable configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	WDT_EN	Watchdog timing enable configuration register, when the

		configuration value is 0x55. the watchdog is closed

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: Interrupt enable; 0: Interrupt disable;

IRCON1 (F1H) Interrupt flag register 1

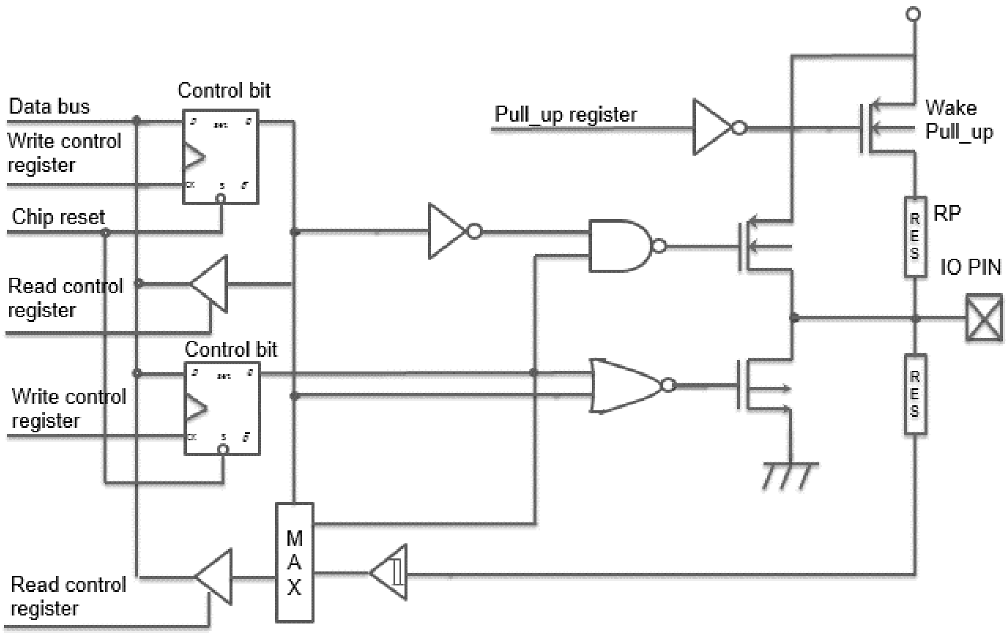
Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: With interrupt flag 0: No interrupt flag

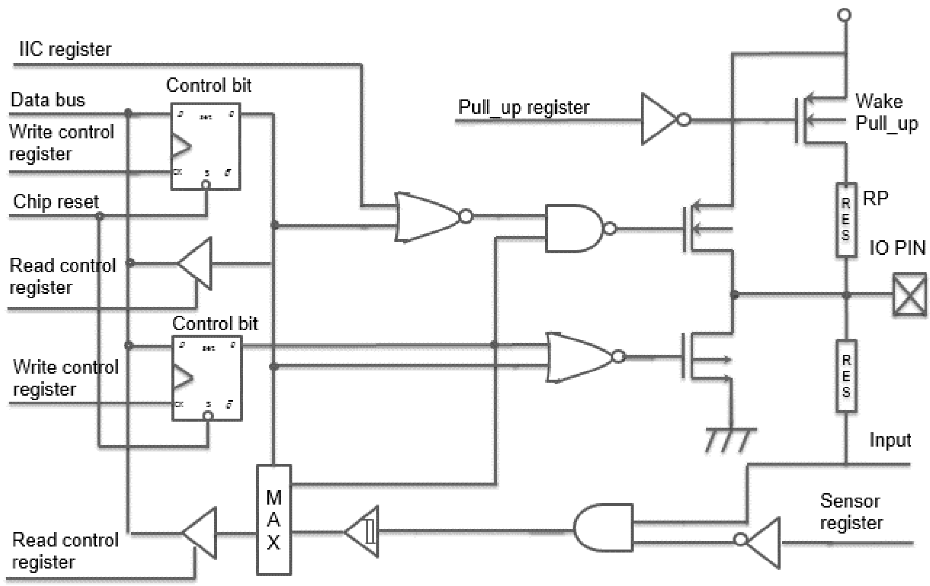
6. GPIO

6.1. GPIO Function Describe

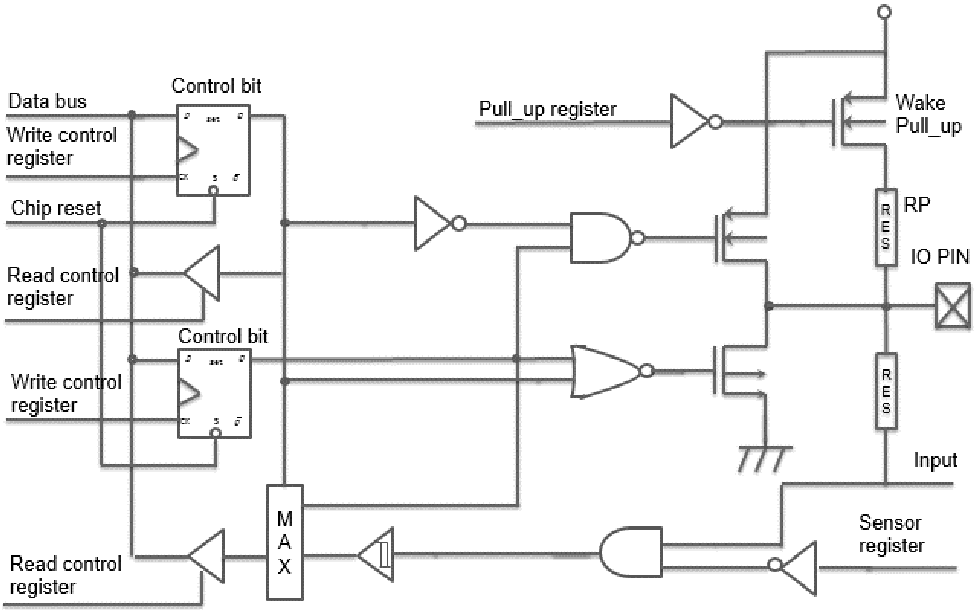
Some pins of the GPIO port are multiplexed with device peripheral functions, and cannot be configured as multiple clock functions at the same time, otherwise it will cause malfunction. IIC communication port, open-drain output, pull-up resister required.



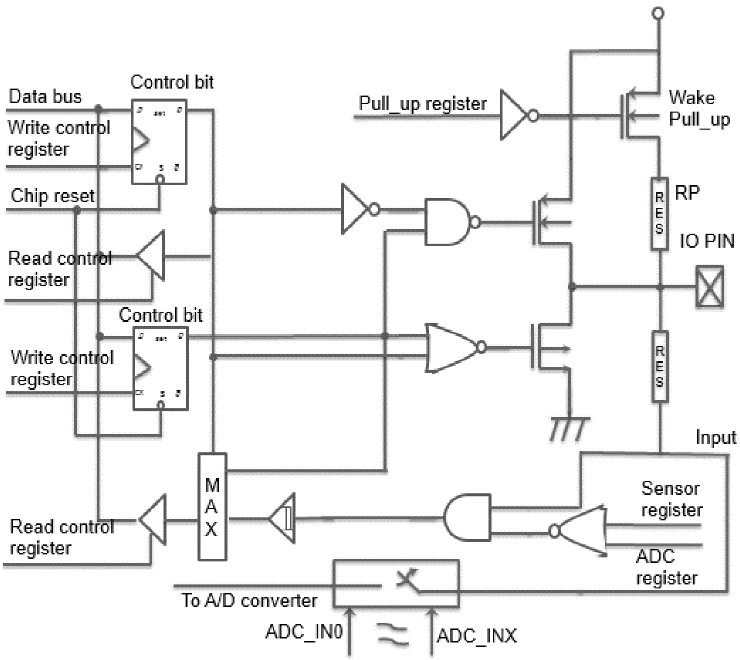
General IO structure



Open-drain output structure



SNS IO structure



ADC IO structure

TRISX register (Direction Register): TRISX set to 1 can be configured as input pin, set to 0 can be configured as output pin.

DATAX register (Data Register): DATAX set to 1 the data in DATAX will be configured as high, set to 0 the data in DATAX will be configured as low.

PU_PX register (pull-up resistor enable register): When PU_PX is set to 1, the corresponding pin pull-up resistor is enabled, and the corresponding pin is cleared to disable the pull-up resistor.

PB pull-up resistor 28k, other IO port pull-up resistor 4.7k.

PD_PB register (PB pull-down resistor enable register): The pull-down resistor of the pin corresponding to PD_PB is set to 1, and the pull-down resistor is not enabled for the pin corresponding to clearing. The built-in pull-down resistor is 28k.

ODRAIN_EN register: Set ODRAIN_EN to 1 to enable open-drain output on the corresponding pin. Clear it to disable open-drain output. After enabling IIC function, open-drain output is automatically turned on. IIC/UART recommends using external pull-up resistors.

Supports high current drive function of 8 GPIO ports.

6.2. GPIO Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xF8	DATAA	RW	xxxx_xx11b	PA data register
0x80	DATAB	RW	1111_1111b	PB data register
0x90	DATAC	RW	1111_1111b	PC data register
0x98	DATAD	RW	1111_1111b	PD data register
0xB0	DP_CON	RW	xxx0_0000b	LED scan control register
0xD8	PD_PB	RW	0000_0000b	PB port pull-down resistor enable register
0xDD	PU_PA	RW	xxxx_xx00b	PA port pull-up resistor enable register
0xDE	PU_PB	RW	0000_0000b	PB port pull-up resistor enable register
0xDF	PU_PC	RW	0000_0000b	PC port pull-up resistor enable register
0xE2	PU_PD	RW	0000_0000b	PD port pull-up resistor enable register
0xEA	TRISA	RW	xxxx_xx11b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_1111b	PC direction register
0xED	TRISD	RW	1111_1111b	PD direction register
0xEE	COM_IO_SEL	RW	0000_0000b	COM port selection configuration register
0xEF	ODRAIN_EN	RW	xxxx_x000b	PA0/PA1/PD6 port open drain output enable register

Port configuration SFR register list

6.2.1. Data registers

DATAA (F8H) PA data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PA1	PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA data register, you can configure the output level of the PA group IO port as GPIO port, the read value is the current level state of the IO port (input) or the configured output value (output)

DATAB (80H) PB data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB data register, configurable PB group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

DATAC (90H) PC data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register, you can configure the output level when the IO port of the PC group is used as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

DATAD (98H) PD data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD data register you can configure the output level when the IO port of the PD group is used as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

6.2.2. Pull-up Resistor Enable Register

PU_PA (DDH) PA port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PU_PA1	PU_PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	PU_PAn n=1~0	PA port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

PU_PB (DEH) PB port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PB7	PU_PB6	PU_PB5	PU_PB4	PU_PB3	PU_PB2	PU_PB1	PU_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PBn n=7~0	PB port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

PU_PC (DFH) PC port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PC7	PU_PC6	PU_PC5	PU_PC4	PU_PC3	PU_PC2	PU_PC1	PU_PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PCn n=7~0	PC port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

PU_PD (E2H) PD port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PU_PD7	PU_PD6	PU_PD5	PU_PD4	PU_PD3	PU_PD2	PU_PD1	PU_PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PU_PDn n=7~0	PD port pull-up resistor enable register 1: Pull-up resistor enabled; 0: Pull-up resistor disabled

6.2.3. Direction Register

TRISA (EAH) PA direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	Bit[1]~ Bit[1]: PA1~PA0 direction of port pins 0: PAx port is output; 1: PAx port is input

TRISB (EBH) PB direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: PB7~PB0 direction of port pins 0: PBx port is output; 1: PBx port is input

TRISC (ECH) PC direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: PC7~PC0 direction of port pins 0: PCx port is output; 1: PCx port is input

TRISD (EDH) PD direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: PD7~PD0 direction of port pins 0: PDx port is output; 1: PDx port is input

6.2.4. Large Current Sink

DP_CON (B0H) LED scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	DUTY_SEL			SCAN_MODE	COM_MOD
R/W	-	-	-	R/W			R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
0	COM_MOD	High current sink IO port drive enable 1: The COM locking function, as large current IO mouth work; 0: The COM port is not locked and can be configured for other functions When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED scan configuration is invalid

COM_IO_SEL (EEH) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, corresponding to PB port 1: Select COM port mode; 0: Select IO port mode

6.2.5. Open Drain Enable Registers

ODRAIN_EN (EFH) PA0/PA1/PD6 port open drain output enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2	--	PD6 open drain output enable register 1: Open drain output; 0: CMOS output
1	--	PA1 open drain output enable register 1: Open drain output; 0: CMOS output
0	--	PA0 open drain output enable register 1: Open drain output; 0: CMOS output

6.2.6. Pull-down Resistor Enable Registers

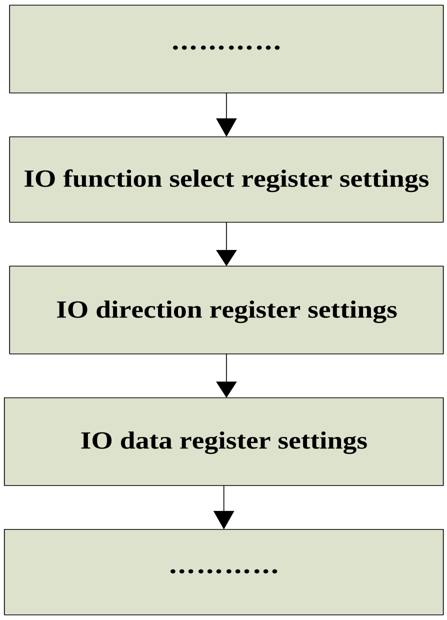
PD_PB (D8H) PB port pull-down resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD_PB7	PD_PB6	PD_PB5	PD_PB4	PD_PB3	PD_PB2	PD_PB1	PD_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PD_PBn (n=7~0)	PB port pull-down resistor enable register 1: Pull-down resistor enabled; 0: Pull-down resistor disabled;

6.3. GPIO Configuration Process

When setting the port as GPIO, the following three sets of registers need to be set accordingly.



IO configuration flow chart

Note:

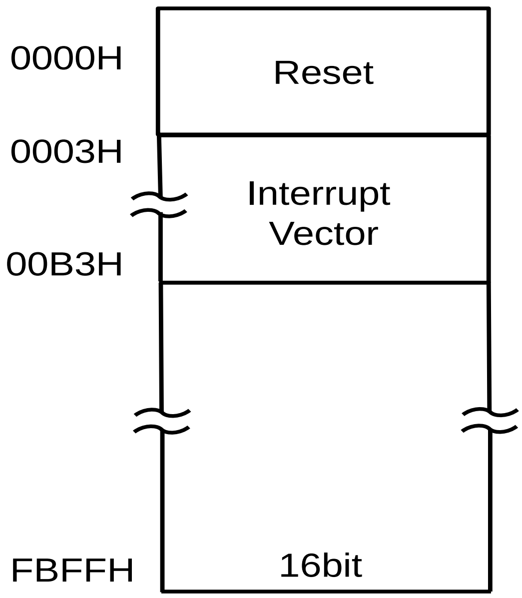
The default source current driving capacity of IO port is typically 18.5mA, and the irrigation current driving capacity is typically 68mA @5V 0.9vcc. When using IO to drive LED/digital tube, it is necessary to pay attention to the Ifp current of LED lamp. It is recommended to add current limiting resistance to limit the peak current of IO drive within the Ifp current of LED/digital tube. If you want to save resistance due to cost, it is recommended to use our unique LED serial dot matrix Module to drive LED/ digital tube.

7. Interrupt

7.1. Interrupt Sources and Entry Address

Interrupt source	Condition	Sign	Enable control	Priority control	Interrupt vector	Query priority	Interrupt number	Flag removal method	wake up low power
INT0	External Interrupt 0 Conditions is met	IE0	IEN0[0]	IPL0[0]	0x0003	1	0	User must clear	Yes
Timer0	Timer0 overflow	TF0	IEN0[1]	IPL0[1]	0x000B	2	1	User must clear	No
INT1	External Interrupt1 Conditions is met	IE1	IEN0[2]	IPL0[2]	0x0013	3	2	User must clear	Yes
Timer1	Timer1 overflow	TF1	IEN0[3]	IPL0[3]	0x001B	4	3	User must clear	No
INT2	External Interrupt2 Conditions is met	IE2	IEN1[2]	IPL1[2]	0x004B	5	9	User must clear	Yes
IIC	Receive or transmit completed	IE3	IEN1[3]	IPL1[3]	0x0053	6	10	User must clear	Yes
ADC	ADC conversion completed	IE4	IEN1[4]	IPL1[4]	0x005B	7	11	User must clear	No
CSD	Counter overflow	IE5	IEN1[5]	IPL1[5]	0x0063	8	12	User must clear	No
LED	Scan complete	IE6	IEN1[6]	IPL1[6]	0x006B	9	13	User must clear	No
WDT/ Timer2	WDT/Timer2/ PWM0 overflow	IE7	IEN1[7]	IPL1[7]	0x0073	10	14	User must clear	Yes
LVDT	Voltage Conditions meet	IE8	IEN2[0]	IPL2[0]	0x007B	11	15	User must clear	V
UART0	Receive or transmit completed	IE9	IEN2[1]	IPL2[1]	0x0083	12	16	User must clear	No
UART1	Receive or transmit completed	IE10	IEN2[2]	IPL2[2]	0x008B	13	17	User must clear	No
INT3	External Interrupt 3 Conditions is met	IE11	IEN2[3]	IPL2[3]	0x0093	14	18	User must clear	Yes

List of interrupt information



When the chip generates a reset signal, the program starts from the 0x0000 address. When an interrupt signal occurs, the program will jump to the interrupt vector program address to execute the interrupt service routine.

7.2. Interrupt Function

7.2.1. Interrupt Response

When an interrupt request, CPU according to the interrupt vectors determine the type of interrupt service routine (ISR) to run. CPU complete execution ISR, unless a higher priority interrupt source applying for a break. After each ISR has RETI (return from interrupt) instruction. After RETI instruction, CPU continues to execute the program before the interrupt did not happen.

ISR can only be a higher priority interrupt request interrupt. That is, the low-priority ISR can be interrupted by a high-priority interrupt request.

The BF7612DMXX-SJLX responses interrupt request until the current instruction finished. If the RETI instruction is being executed or read IP, IEN register, after an additional instruction then respond the interrupt request.

7.2.2. Interrupt Priority

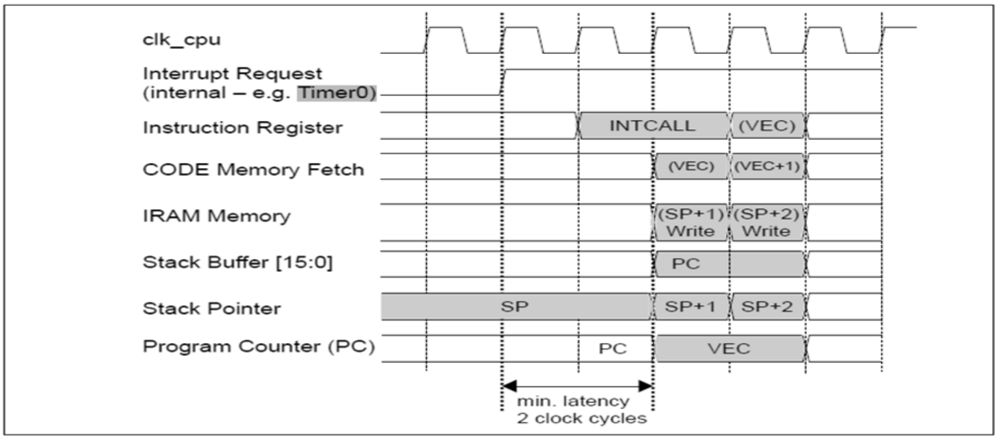
The BF7612DMXX-SJLX has two interrupt priority levels: interrupt level and the default priority.Interrupt level (top, high and low) override the default priority. The priority set to high is the first to respond. When the priority is set to the same level, the response will be queued by default. Power-down interrupt is the only high-level interrupt source if allowed. All interrupt sources can be set to high priority or low priority.

Each interrupt source can be assigned a priority level (high or low), and the default priority. The same level of interrupt sources (such as both high priority) the priority is the default priority decision. Interrupt service routine in progress can only be a high-priority interrupt request interrupt.

7.2.3. Interrupt Sample

Internal modules such as internal timers and serial ports generate interrupt requests through interrupt flag bits in their respective SFR. When the first clock cycle (C1) of each instruction cycle ends, the External Interrupt is sampled on the rising edge of the clock.

In order to ensure that the edge-triggered interrupt is detected, the corresponding port must first maintain the high level of 2 clocks, and then keep the low level of 2 clocks. The following figure shows the timing diagram of interrupt sample:



7.2.4. Interrupt Wait

Interrupt response time is determined by current state. Fastest response time is five instruction cycles: one cycle to detect the interrupt request, the other 4 used to execute long call (LCALL) to ISR.

When the system is executing a RETI instruction and is followed by a MUL or DIV instruction, the interrupt waits for the longest time (13 instruction cycles). This 13 instruction cycles are as follows: one cycle to detect the interrupt request, three to complete the RETI, five used to execute DIV or MUL instruction, 4 used to execute long call (LCALL) to ISR. In this case, the response time is 13 clock cycles.

7.3. Interrupt Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status flag
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT power-on/brown-out interrupt status register
0x88	TCON	RW	0000_0x0xb	Timer control register
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC/INT function control register
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	EXT_INT_CON	RW	x001_0101b	External interrupt polarity control register

7.3.1. Interrupt Status Registers

INT_PE_STAT (85H) WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status flag, this bit write 0 to clear zero, write WDT_CTRL operation can also clear 0 1: Interrupt is valid; 0: Interrupt is invalid;
0	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is written 0 to clear, write TIMER2_CFG operation also can clear 1: Interrupt is valid; 0: Interrupt is invalid;

INT_POBO_STAT (86H) LVDT power-on/brown-out interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT

R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	LVDT power-on interrupted stat 1: Power-on interrupt is valid; 0: Power-on interrupt is invalid.
0	INT_BO_STAT	LVDT brown-out interrupt status. 1: Brown-out interrupt is valid; 0: Brown-out interrupt is invalid

7.3.2. Interrupt Enable Registers

IEN0 (A8H) Interrupt enable register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer 1 overflow interrupt enable bit: 0: Disable timer 1 (TF1) to apply for interrupt; 1: Allow TF1 flag bit to request interrupt.
2	EX1	INT_EXT1 enable bit: 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 overflow interrupt enable bit: 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT 0 enable bit: 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0

Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
6	EX6	LEDinterrupt enable 1: Interrupt enable; 0: Interrupt disable;
5	EX5	Reserved
4	EX4	ADC interrupt enable 1: Interrupt enable; 0: Interrupt disable;
3	EX3	IIC interrupt enable 1: Interrupt enable; 0: Interrupt disable;
2	EX2	External Interrupt 2 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
1~0	-	Reserved

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	-	Reserved
3	EX11	External Interrupt 3 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
2	EX10	UART1 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
1	EX9	UART0 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
0	EX8	LVDT interrupt enable 1: Interrupt enable; 0: Interrupt disable;

7.3.3. Interrupt Priority Registers

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1 (Timer1 interrupt) priority selection bit. 0: Low priority; 1: High priority
2	PX2	External interrupt 1 interrupt priority selection bit. 0: Low priority; 1: High priority
1	PT0	TF0 (Timer0 interrupt) priority selection bit. 0: Low priority; 1: High priority
0	PX0	External interrupt 0 interrupt priority selection bit. 0: Low priority; 1: High priority

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IPL2.3	External interrupt 3 interrupt priority 0: Low priority; 1: High priority
2	IPL2.2	UART1 interrupt priority 0: Low priority; 1: High priority
1	IPL2.1	UART0 interrupt priority 0: Low priority; 1: High priority
0	IPL2.0	LVDT interrupt priority 0: Low priority; 1: High priority

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority 0: Low priority; 1: High priority
6	IPL1.6	LED priority 0: Low priority; 1: High priority
5	IPL1.5	CSD interrupt priority 0: Low priority; 1: High priority

4	IPL1.4	ADC interrupt priority 0: Low priority; 1: High priority
3	IPL1.3	IIC interrupt priority 0: Low priority; 1: High priority
2	IPL1.2	External interrupt 2 priority 0: Low priority; 1: High priority
1~0	--	Reserved

7.3.4. Interrupt Flag Registers

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	IE11	External Interrupt 3 interrupt flag 1: With interrupt flag 0: No interrupt flag
2	IE10	UART1 interrupt flag 1: With interrupt flag 0: No interrupt flag
1	IE9	UART0 interrupt flag 1: With interrupt flag 0: No interrupt flag
0	IE8	LVDT interrupt flag 1: With interrupt flag 0: No interrupt flag

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: With interrupt flag 0: No interrupt flag
6	IE6	LED interrupt flag 1: With interrupt flag 0: No interrupt flag
5	IE5	CSD interrupt flag 1: With interrupt flag 0: No interrupt flag
4	IE4	ADC interrupt flag

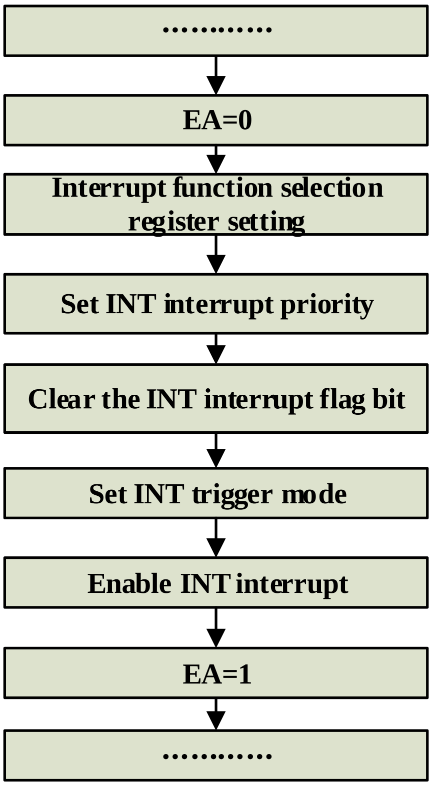
		1: With interrupt flag　0: No interrupt flag
3	IE3	IIC interrupt flag 1: With interrupt flag　0: No interrupt flag
2	IE2	External interrupt 2 interrupt flag 1: With interrupt flag　0: No interrupt flag
1~0	--	Reserved

7.4. External Interrupt

7.4.1. Features

- All IO ports support external interrupt
- INT0~2 external interrupt (rising edge, falling edge, double edge), INT3 shared interrupt source (rising edge, falling edge)
- INT3 shares one interrupt vector, and can only respond to one external interrupt at the same time. When the rising or falling edge of the external interrupt on multiple pins is enabled, all the external interrupt pins must be released during the detection process to respond to the current trigger signal. (When the falling edge is triggered, the release is high, and when the rising edge is triggered, the release is low)

7.4.2. Configuration Process



INT configuration flow chart

7.4.3. Registers

7.4.3.1. IIC Function Control Register

PERIPH_IO_SEL (F2H) IIC/INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	-	-
R/W	-	R/W	R/W	-	-
Reset value	-	1	0	-	-
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
2	INT2_IO_SEL	INT2 port selection enable 1: Select INT2 function; 0: Not select INT2 function
1	INT1_IO_SEL	INT1 port selection enable 1: Select INT1 function; 0: Not select INT1 function
0	INT0_IO_SEL	INT0 port selection enable 1: Select INT0 function; 0: Not select INT0 function

7.4.3.2. External Interrupt Polarity Control Register

EXT_INT_CON (F7H) External interrupt polarity control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	INT3_POLARITY	INT2_POLARITY		INT1_POLARITY		INT0_POLARITY	
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	0	1	0	1	0	1

Bit number	Bit symbol	Description
6	INT3_POLARITY	External Interrupt 3 trigger polarity selection: 0: Falling edge (low-level wake-up in Sleep mode) 1: Rising edge (high level wake-up in Sleep mode)
5~4	INT2_POLARITY	External Interrupt 2 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
3~2	INT1_POLARITY	External Interrupt 1 trigger polarity selection:

		01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
1~0	INT0_POLARITY	External Interrupt 0 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)

7.4.3.3. INT3 Select Enable Registers

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x25	PERIPH_IO_SEL3	RW	x000_0000b	INT3 select enable register 3
0x26	PERIPH_IO_SEL2	RW	0000_0000b	INT3 select enable register 2
0x27	PERIPH_IO_SEL1	RW	0000_0000b	INT3 select enable register 1

PERIPH_IO_SEL3 (25H) INT3 select enable register 3

Bit number	7	6	5	4
Symbol	-	INT3_22_IO_SEL	INT3_21_IO_SEL	INT3_20_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	INT3_19_IO_SEL	INT3_18_IO_SEL	INT3_17_IO_SEL	INT3_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~0	INT3_n_IO_SEL (n=22~16)	INT3_n port selection enable 1: Select INT function 0: Not select INT function

PERIPH_IO_SEL2 (26H) INT3 select enable register 2

Bit number	7	6	5	4
Symbol	INT3_15_IO_SEL	INT3_14_IO_SEL	INT3_13_IO_SEL	INT3_12_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_11_IO_SEL	INT3_10_IO_SEL	INT3_9_IO_SEL	INT3_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=15~8)	INT3_n port selection enable 1: Select INT function 0: Not select INT function

PERIPH_IO_SEL1 (27H) INT3 select enable register 1

Bit number	7	6	5	4
Symbol	INT3_7_IO_SEL	INT3_6_IO_SEL	INT3_5_IO_SEL	INT3_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_3_IO_SEL	INT3_IO_2_SEL	INT3_1_IO_SEL	INT3_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=7~0)	INT3_n port selection enable 1: Select INT function 0: Not select INT function

8. Timer

8.1. General Description

The BF7612DMXX-SJLX series contains 3 timers Timer0, Timer1. Timer2. Each Timer contains a 16-bit register. When accessed, it appears in the form of two bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The registers of Timer2 are the low byte TIMER2_SET_L and the high byte TIMER2_SET_H.

The function features of Timer are as follows:

- Timer0 is connected to system clock, and the timing clock is divided by F_sys_clk/12;
- Timer1 is connected to system clock, and the timing clock is divided by F_sys_clk/12;
- Timer2 can choose LIRC 32kHz or external crystal clock, frequency 32768Hz/4MHz;
- Timer0 supports 8bits automatic reload timing, 16bits manual reload timing function;
- Timer1 supports 8bits automatic reload timing, 16bits manual reload timing function;
- Timer2 supports 32bits automatic reload timing and manual reload timing, and supports interrupt wake-up function.

8.2. Timer0 and Timer1

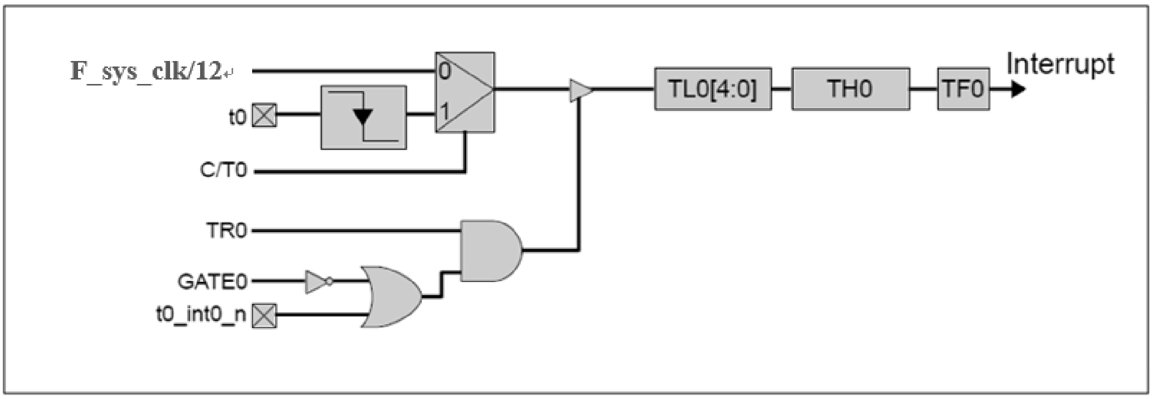
8.2.1. Overview

Timer0 is enabled by setting ET0 bit in the IEN0 register, and Timer1 is enabled by setting ET1 bit in the IEN0 register. By setting tr0/1 bit in the TCON register to enable the counter to work, and tf0/1 bit to determine whether the timer overflow interrupt. Timer 0/1 has four operating modes, controlled by TMOD SFR and TCON SFR.

The four modes of Timer 0/1 are as follows:

- 13-bit timer (Mode 0)
- 16-bit timer (Mode 1)
- Automatically reloads an 8-bit timer at initial values (Mode 2)
- Two 8-bit timers (Mode 3, only for timer 0)

Mode 0: 13-bit timer

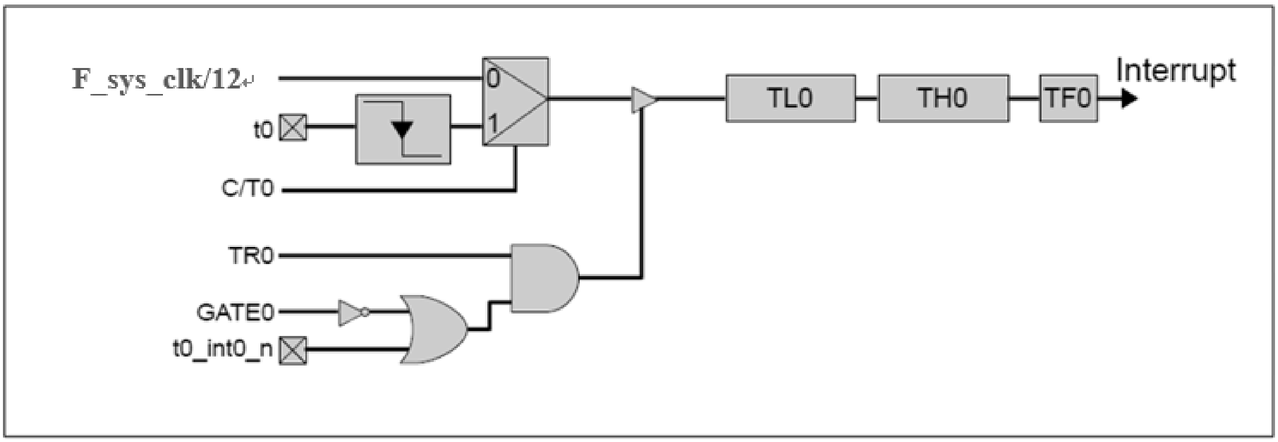


Mode 0 logical structure diagram

As shown in the figure, the working process of timer 0 and timer 1 is the same. In mode 0, Timer 0 is a 13-bit counter, and the 13-bit register consists of 8 bits of TH0 and the lower 5 bits of TL0. Timer 1 is a 13-bit counter, and the 13-bit register consists of 8 bits of TH1 and the lower 5 bits of TL1. The upper three bits of TL0 and TL1 should be ignored. The enable bit (TR0/TR1) in the TCON register controls the on and off of the timer.

The timer counts the selected System clock source (sys_clk/12). When the 13-bit counter counts up to all 1, the counter is cleared to 0 (all 0), and TF0 (or TF1) is set. In mode 0, the upper 3 bits of TL0 (or TL1) are indeterminate, and these 3 bits should be masked out or ignored when the R count value. T0/t1, C/T0, C/T1 are all 0, t0_int0_n/ t1_int1_n are all 1. and the count enable is only determined by TR0/1.

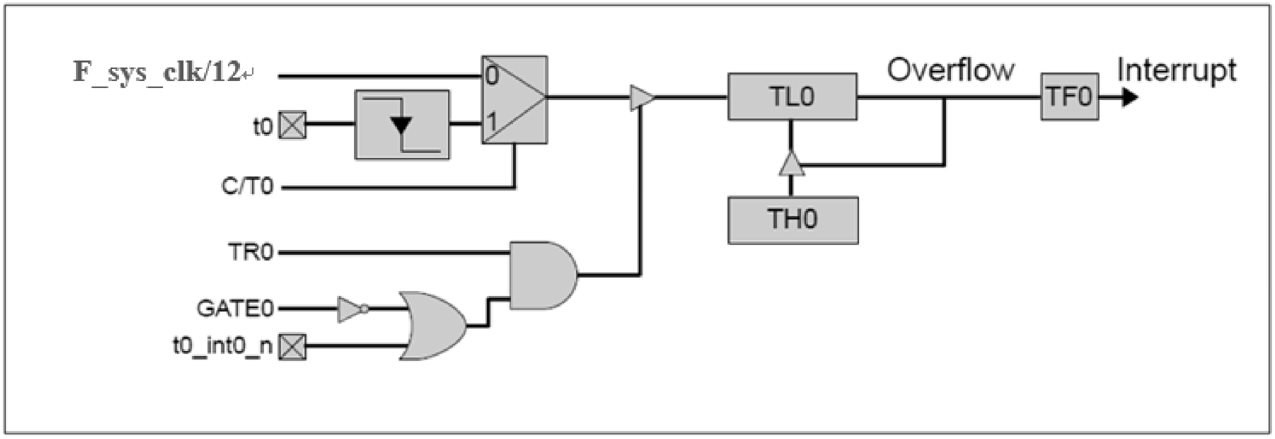
Mode 1: 16-bit timer



Mode 1 logical structure diagram

As shown in the figure, Mode 1 of Timer 0 and Timer 1 are the same. In Mode 1. The timer is a 16-bit counter. All 8 bits of the LSB register (TL0 or TL1) are used. When the timer counts up to 0Xffff, the counter is cleared to all 0. Other than that, Mode 1 and Mode 0 are the same. T0/t1. C/T0, C/T1 are all 0, t0_int0_n/ t1_int1_n are all 1. And the count enable is only determined by TR0/1.

Mode 2: 8-bit timer with automatic reloading of initial value

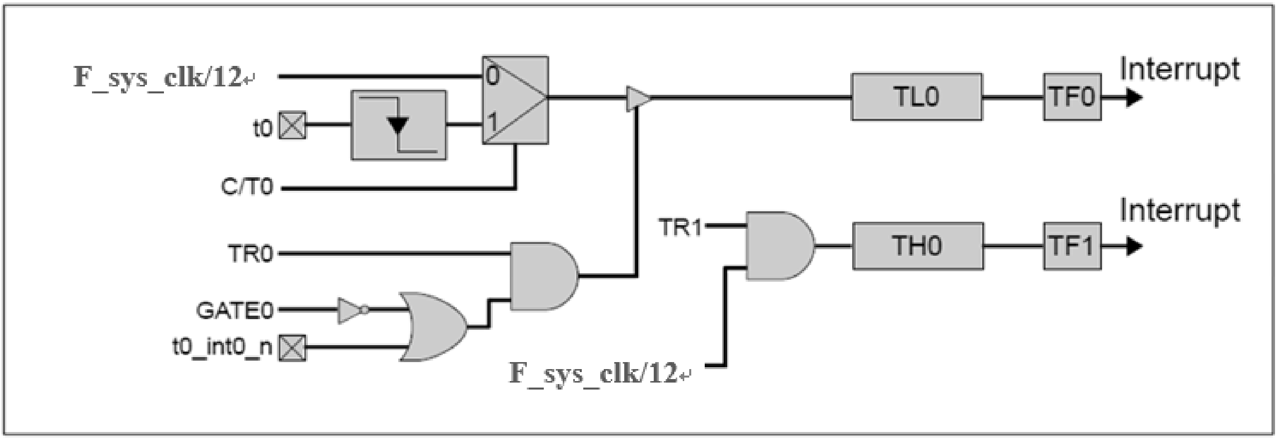


Mode 2 logical structure diagram

Mode 2 of Timer 0 and Timer 1 are the same. In mode 2. The timer is an 8-bit counter with an automatic reload initial value. This counter is the LSB register (TL0 or TL1), and the initial value that needs to be reloaded is stored in the MSB register (TH0 or TH1).

As shown in the figure, the counter control of Mode 2 is the same as Mode 0 and Mode 1. However, in mode 2. When TLn accumulates to FFh, the value stored in THn is reloaded to TLn. T0/T1, C/T0, C/T1 are all 0, t0_int0_n/t1_int1_n are all 1. And counting enable is only determined by TR0/1.

Mode 3: Two 8-bit timers



Mode 3 logical structure diagram

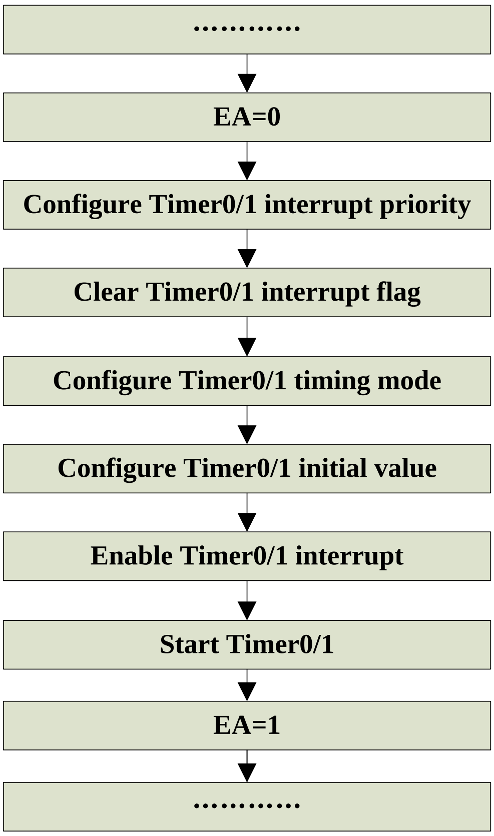
In mode 3. Timer 0 is two 8-bit timers, at this time Timer 1 stops counting and saves its value. As shown in Figure 5. TL0 is an 8-bit register controlled by the timer 0 control bit. The counter uses GATE as the enable terminal to control the INT_EXT signal reception.

TH0 is a separate 8-bit timer. TH0 can only be used to calculate the clock period (divide by 12). The control bit and flag bit (TR1 and TF1) of Timer 1 are used as the control bit and flag bit of TH0.

When Timer 0 works in Mode 3. The use of Timer 1 is restricted, because Timer 0 uses the control bit (TR1) and interrupt flag (TF1) of Timer 1. Timer 1 can still be used to generate the baud rate, and the value of Timer 1 in the TL1 and TH1 registers is still valid.

When timer 0 works in mode 3. Timer 1 is controlled by the mode bit of timer 1. To start timer 1. You need to set timer 1 to mode 0, 1 or 2. To turn off timer 1. Set the mode of timer 1 to 3. Timer 1 can be used as a timer (clock is clk/12), but because TR1 and TF1 are borrowed, overflow interrupts cannot be generated. When timer 0 is working in mode 3. The GATE of timer 1 is valid. T0/T1, C/T0, C/T1 are all 0, t0_int0_n/t1_int1_n are all 1. And counting enable is only determined by TR0/1.

8.2.2. Timer0/1 Configure Process



Timer0/1 configure process

8.2.3. Timer0/1 Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x88	TCON	RW	xx00_xx00b	Timer control register
0x89	TMOD	RW	0000_0000b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 timer low 8 bits
0x8B	TL1	RW	0000_0000b	Timer 1 timer low 8 bits
0x8C	TH0	RW	0000_0000b	Timer 0 timer high 8 bits
0x8D	TH1	RW	xx00_xx00b	Timer 1 timer high 8 bits
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register 0
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0

Timer0/1 SFR register list

8.2.3.1. Timer Control Register

TCON (88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
6	TR1	Timer1 start enable, when set to1, start Timer1. Or start Time0 mode three, TH0 count.
5	TF0	Timer 0 overflow flag, set by hardware when Timer0 overflows.
4	TR0	Timer0 start enable, set to 1 to start Timer0 counting.

8.2.3.2. Timer Mode Register

TMOD (89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved

5~4	M1[1:0]	Timer 1 mode select bit 00: Mode 0 - 13-bit timer 01: Mode 1 - 16-bit timer 10: Mode 2 - 8-bit timer with automatic reloading of initial value 11: Mode 3 - Two 8-bit timers
1~0	M0[1:0]	Timer 0 mode select bit 00: Mode 0 - 13-bit timer 01: Mode 1 - 16-bit timer 10: Mode 2 - 8-bit timer with automatic reloading of initial value 11: Mode 3 - Two 8-bit timers

8.2.3.3. Timer 0 Timer Registers

TL0 (8AH) Timer 0 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TH0 (8CH) Timer 0 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

8.2.3.4. Timer 1 Timer Registers

TL1 (8BH) Timer 1 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH1 (8DH) Timer 1 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

8.2.3.5. Interrupt Related Registers

IEN0 (A8H) Interrupt enable register 0

Bit number	7	6	5	4	3	2	1	0

Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
3	ET1	Timer 1 overflow interrupt enable bit: 0: Disable timer 1 (TF1) to apply for interrupt; 1: Allow TF1 flag bit to request interrupt.
1	ET0	Timer 0 overflow interrupt enable bit: 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	PT1	TF1 (Timer1 interrupt) priority selection bit. 0: Low priority; 1: High priority
1	PT0	TF0 (Timer0 interrupt) priority selection bit. 0: Low priority; 1: High priority

8.3. Timer2

8.3.1. Overview

Timer2 module plays a timing role. The internal main structure of the Timer2 module is a 16-bit counter. The timer function is achieved by counting the input clock. The counting principle of Timer2 is accumulative counting. An interrupt is generated when the count reaches the set value. Timer2 count clock can choose external XTAL and internal low-speed clock LIRC. TIMER2 has two working modes: single timer mode and auto-reload mode. In either mode, an interrupt will be generated when the timer is completed.

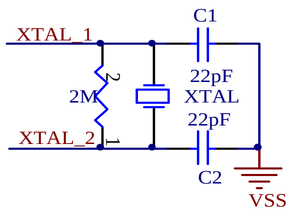
Configure Timer2 function enable through register TIMER2_EN, TIMER2_RLD configure automatic reload mode or manual reload mode, the timing time is determined by registers TIMER2_SET_L and TIMER2_SET_H. The timing clock can be selected from the internal low-speed clock LIRC 32kHz or the external crystal clock with a frequency of 32.768kHz/4MHz, which is determined by the clock selection register.

Timer2 supports interrupt wake-up low-power mode function, and software needs to clear the interrupt flag in the interrupt processing function.

Timer2 timing duration formula:

$T_{TIMER2}=T_{TIMER2\_CLK}*(\{TIMER2\_SET\_H, TIMER2\_SET\_L\}+1)$

Note: T_{TIMER2_CLK} = 1/32768 (s) or T_{TIMER2_CLK} = 1/4M (s)

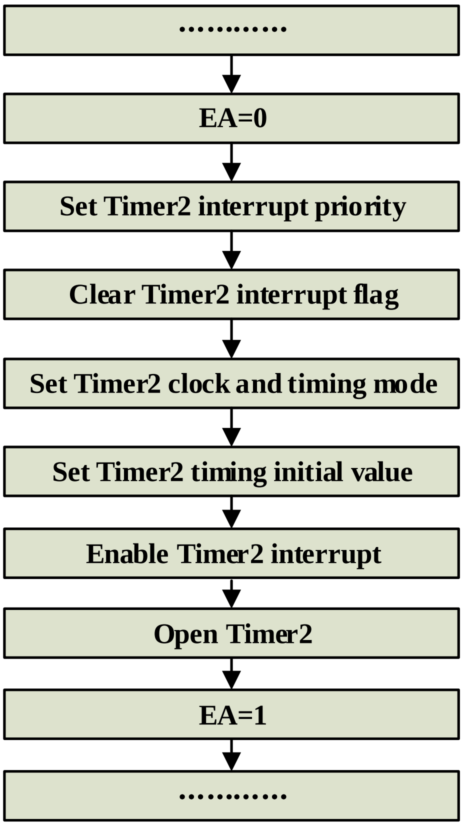


External crystal oscillator circuit reference

Note:

1. Any configuration of TIMER2_SET_H, TIMER2_SET_L, TIMER2_CFG can clear the counter;
2. External crystal oscillator circuit is for reference only, the actual Parameter refers to the crystal oscillator specifications;

8.3.2. Timer2 Configure Process



Timer2 configure process table

During the configuration flow:

1. First configure the timing set value registers TIMER2_SET_H/TIMER2_SET_L;
2. Then configure the automatic reload enable register TIMER2_RLD as needed, set it to 1 if automatic loop count is required, otherwise configure it to 0;
3. Finally, configure the timing enable register TIMER2_EN and turn on the timing configuration TIMER2_EN=0x1;
4. Stop timing: TIMER2_EN=0x0.

Note:

1. TIMER2_EN=0x1 operation should be placed at the end of all configurations;
2. During the timing of TIMER2. It is forbidden to change the related configuration of Timer2. If you want to modify it, you need to stop the timing first.
3. For precise timing, in the automatic reload mode, the three registers of TIMER2 are not allowed to be configured during interrupt processing.

8.3.3. Timer2 Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status flag
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 count value configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 count value configuration register, low 8 bits
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xx00_0111b	Module switch control register

Timer2 SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x20	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal clock selection register

8.3.3.1. TIMER2 Configuration Register

TIMER2_CFG (93H) TIMER2 configuration register

Bit number	7~3	2	1	0
Symbol	-	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	TIMER2_CLK_SEL	Timer2 clock selection register 1: Select XTAL 0: Select LIRC
1	TIMER2_RLD	TIMER2 auto reload enable register 1: Auto reload mode; 0: Manual reload mode
0	TIMER2_EN	TIMER2 count enable register Configure 1 to start timing, configure 0 to stop timing; In manual reload mode, the hardware will automatically clear this register after the count is completed, stop

		counting, and in automatic reload mode, the enable register will be maintained after the count is completed, and it will automatically restart; Counting from zero, no matter which mode, if this register is set to 1 during the counting process, it will start counting from zero.

8.3.3.2. TIMER2 Count Value Configuration Registers

TIMER2_SET_H (94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_H[7:0]	TIMER2 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER2_SET_L (95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_L[7:0]	TIMER2 count value configuration register, low 8 bits, the register will count again when configured during scanning.

8.3.3.3. Interrupt Related Registers

INT_PE_STAT (85H) WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
0	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is written 0 to clear, write TIMER2_CFG operation also can clear

		1: Interrupt is valid; 0: Interrupt is invalid;

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: Interrupt enable; 0: Interrupt disable;

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: With interrupt flag 0: No interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority 0: Low priority; 1: High priority

8.3.3.4. Module Switch Control Register

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
7~5	--	Reserved
2	PD_XTAL_32K	RTC crystal circuit (32768Hz/4MHz) control register 1: Closed, 0: Open, closed by default

8.3.3.5. Crystal Clock Selection Register

Secondary bus register

XTAL_CLK_SEL (20H) Crystal clock selection register

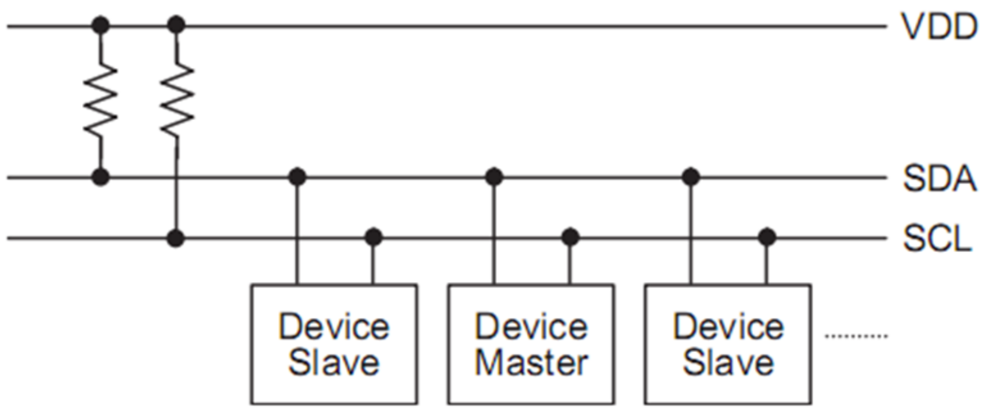
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	XTAL_CLK_SEL
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	XTAL_CLK_SEL	RTC crystal circuit selection register 1: XTAL 4MHz; 0: XTAL 32768Hz

9. IIC

The BF7612DMXX-SJLX supports standard and fast IIC communication, and has the following characteristics:

- Two serial interfaces: serial data line SDA and serial clock line SCL
- Comply with philips standard communication protocol
- Transmission rate: 100Kbps, 400Kbps
- Support 7-bit address addrring
- With the function of extending the low level of the clock
- The core can be awakened by IIC interrupt in low_ power mode
- Detect write conflicts and abnormal buffer BUF overflow



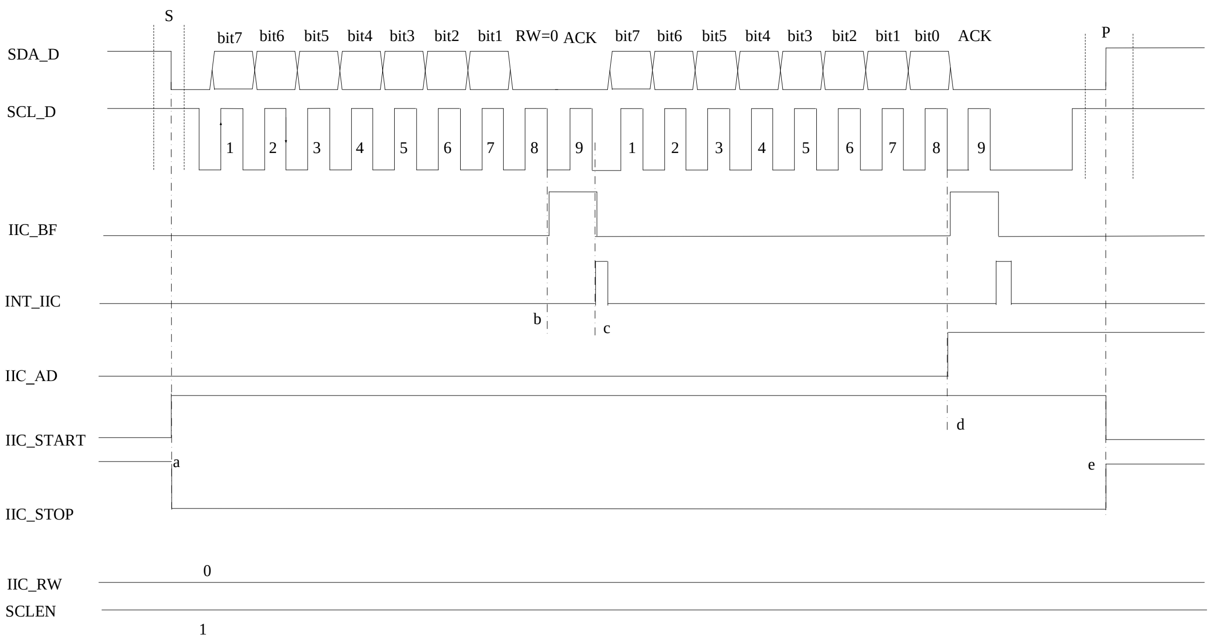
IIC master-slave connection diagram

The master and slave are connected by SCL (serial clock) line and SDA (serial data) line. In IIC communication mode, PA0/1 are open-drain, and SCL and SDA must be connected to a pull resistor (4.7K to 10K is recommended). When the TS device has touch-related actions, such as touch, slide, finger away and other gestures, the host can obtain the touch state of the slave through IIC communication.

9.1. Communication Timing

The BF7612DMXX-SJLX uses hardware slave. When host read /write data, after the slave receives the address, if the address matches, an interrupt is generated and a valid response signal is sent. And an interrupt is generated after the host computer writes the 8h clock of the data, and the host will not generate an interrupt signal when sending the stop signal. IIC timing diagram as follows:

IIC host write timing diagram



IIC write not pull down clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled down during the host write operation. From this, you can see the changes of the IIC bus and some internal signal changes.

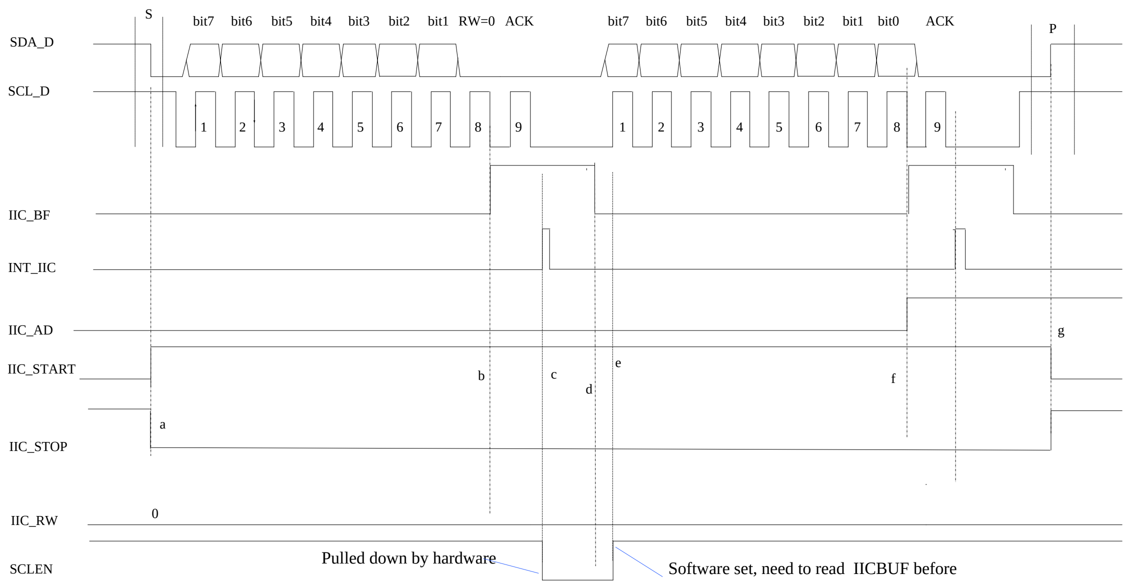
First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a in the figure.

Then the host sends the address bytes and RW flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the 8h clock if the address matches, as shown by the dotted line b in the figure.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c. The MCU executes interrupt subroutine device needs to read IICBU. Even if this data is not useful. Reading the IICBUF operation will indirectly clear the START_BF. The host continues to send messages. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set. The currently received byte of the flag is data, as shown by the dotted line d. The stop signal has no effect on the IIC_AD flag. That is, the stop signal IIC_STOP is detected, and the IIC_AD flag will not be cleared; The interrupt is generated after the falling edge of the ninth clock, and the interrupt subroutine requires the same operation. If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host write pull low timing diagram



IIC write low clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a.

Then the host sends the address bytes and RW flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the 8h clock if the address matches, as shown by the dotted line b in the figure. An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c.

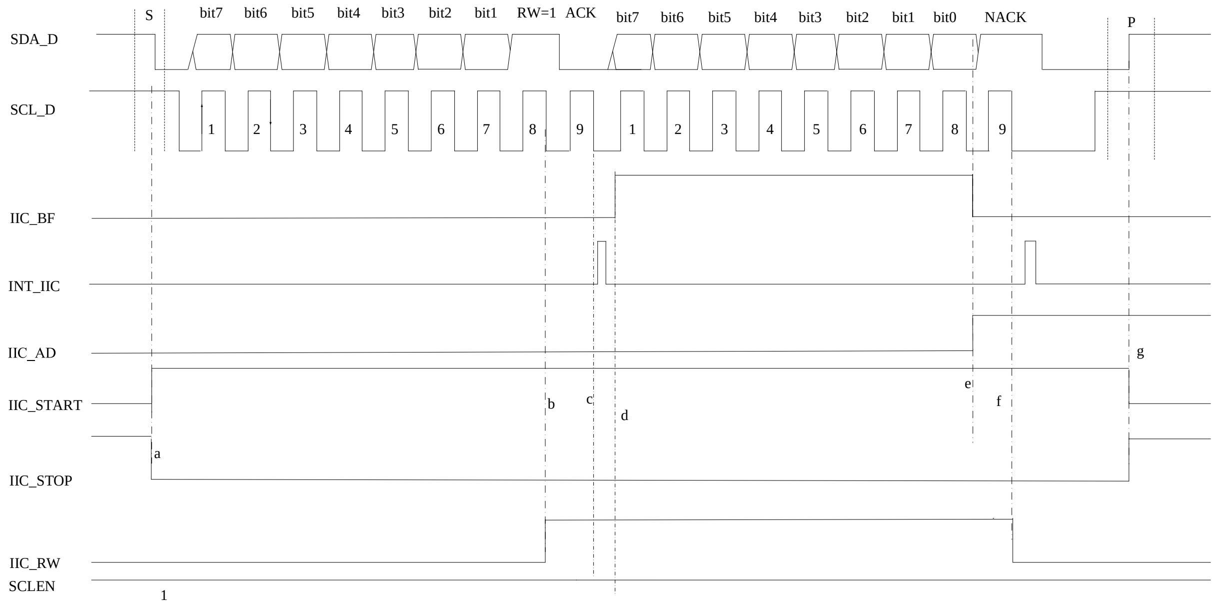
SCLEN will be automatically cleared by hardware after the falling edge of the 9th clock. This process is used to process or read data from the slave. Even if this data is not useful, reading IICBUF will cause IIC_BUF to be cleared indirectly, as shown by the dotted line d. Software sets SCLEN to release the clock line.As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set, the currently received byte of the flag is data, as shown by the dotted line f, and the stop signal has no effect on the IIC_AD flag. That is, the stop signal IIC_STOP is detected, and the IIC_AD flag will not be cleared; The interrupt is generated after the falling edge of the ninth clock.

If the host wants to send multiple bytes, it can continue to send, as shown in the figure above, it only indicates that the host sends one piece of data. The situation that needs to be noted is that when the host sends the last data, the function of pulling down the clock line is not enabled.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host read timing diagram



IIC master reading does not pull down the clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address bytes, IIC_RW = 1, indicates that the host reads the slave. In the case of address match, after the falling edge of the 8h clock, the status bit IIC_RW is set, as shown by the dotted line b; If Address does not match, IIC_RW will not be set.

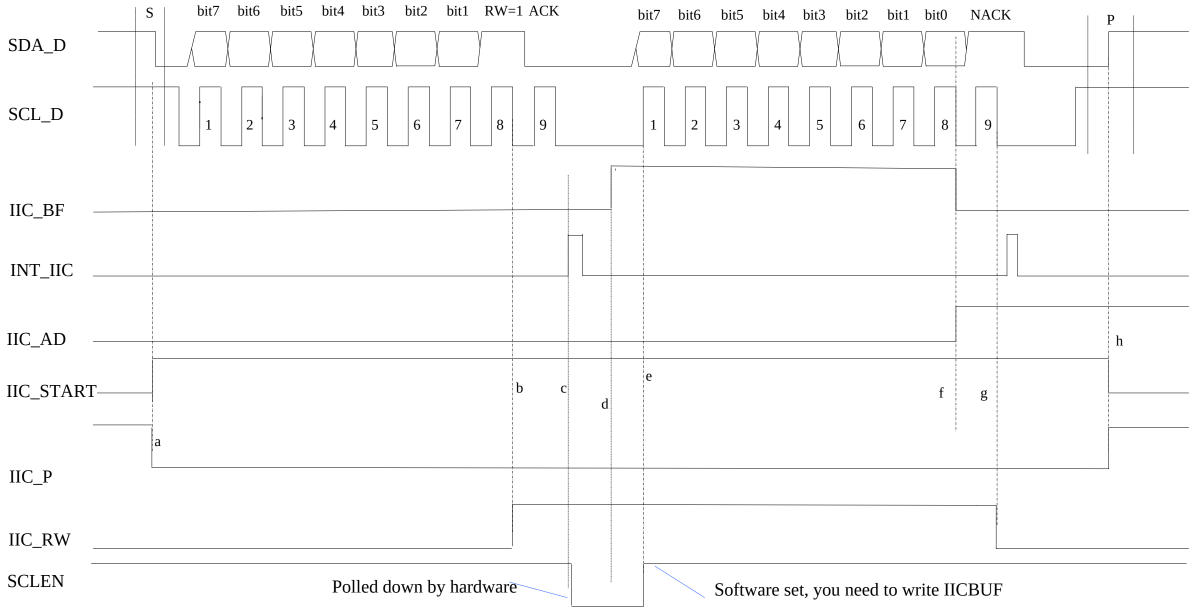
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. Ballast the data in IICBUFFER to IICBUF, IIC is set, as shown by the dotted line d, and the highest bit is sent to the bus. After the 8h clock, one byte of data is sent, IIC_BF is set to clear; At the same time, the address data flag will also be set. As shown by the dotted line e.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate. If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication.

In the diagram, the host only reads one piece of data, and then responds with NACK, and then sends the IIC_STOP signal to terminate the communication.When the NACK is detected, the read/write flag IIC_RW is cleared by hardware. As shown by the dotted line f. If the host sends a NACK, the slave SCLEN will not be automatically pulled low.

Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line g. The bus enters the idle state.

IIC host read pull low timing diagram



IIC host read pull low clock line diagram

As shown in the figure above, it is the timing diagram of the master reading the slave clock line low. From the figure, we can know the changes of the bus and the changes of the internal signals of some circuits.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address byte after the IIC_START signal. IIC_RW = 1, indicates that the host reads the slave. In the case of Address matching, after the falling edge of the 8h clock, status bit IIC_RW set. As shown by the dotted line b. Will not be set if the addresses do not match.

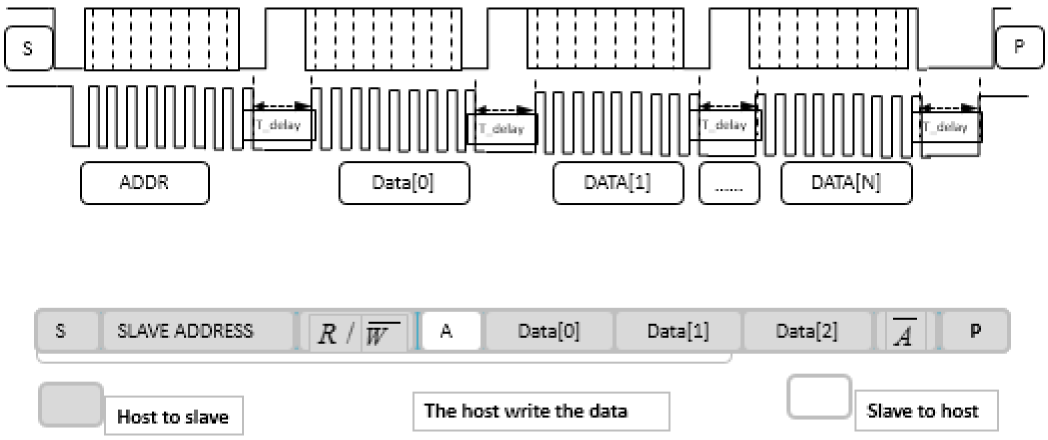
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. SCLEN will also be automatically pulled low by the hardware after the falling edge of the ninth clock. This period is used to process or prepare data from the slave, then write the prepared data to IICBUF, set SCLEN in software, and release the clock line. As shown by the dotted line d. In writing the data to the IICBUF, the IICBUF will be set, indicating that the IIC is full at this time. As shown by the dotted line e. Software sets SCLEN, releases the clock line.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock and read the slave data. After the falling edge of the 8th clock, one byte of data has been sent and IIC_BF cleared; At the same time, the address data flag will also be set, indicating the currently transmitted byte data. As shown by the dotted line f.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to continue to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate; If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. In the diagram, the host reads only one piece of data, replies to NACK, and then sends the IIC_STOP signal to terminate the communication. When the NACK is detected, the read/write flag IIC_RW is cleared by hardware. As shown by the dotted line g.

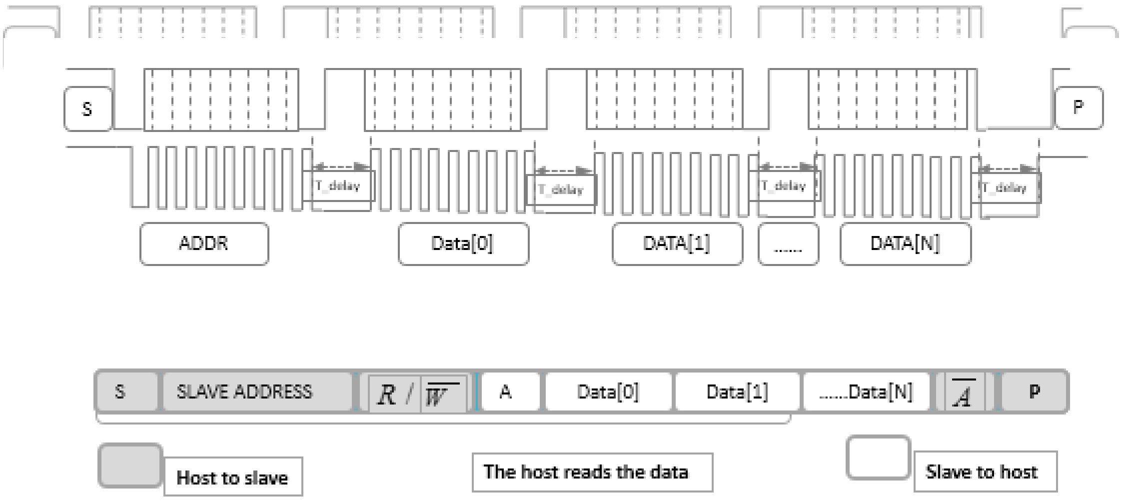
Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line h. The bus enters the idle state.

IIC host write data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us .

IIC host read data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us.

At the 8h clock slave send ack, IIC interrupt occurs at the ninth clock fulling edge. It is recommended that the host delay 60us~300us when the ninth clock fulling edge is sent. Reserve the slave IIC interrupt service data preparation time, and then send the clock signal.

Note: If IIC communication >=100K, it is recommended that system clock 6MHz.

9.2. IIC Port Configuration

The BF7612DMXX-SJLX provides secondary bus register. IIC_IO_SEL Configures IIC mapping IO ports.
For example, configure PA0/PA1 port select IIC function, configure IIC_IO_SEL= 0x00:
PA0: SCL0_A, IIC serial clock line
PA1: SDA0_A, IIC serial data line
Secondary bus register:
IIC_IO_SEL (2CH) IIC mapping IO port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	IIC_IO_SEL[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	IIC_IO_SEL[1:0]	IIC port selection enable 00: PA0/PA1 port select IIC function 01: PB5/PC0 port select IIC function 10: PA1/PD6 port select IIC function 11: Reserved When PB5/PC0 is used as an IIC port, there is no SR control function, and the automatic logic control changes to open leakage output. When PB5/PC0 is GPIO, there is no open leakage output function

9.3. IIC Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit and receive data register
0xE5	IICCON	RW	xx01_0000b	IIC control register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

IIC SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x2C	IIC_IO_SEL	RW	xxxx_xx00b	IIC mapping IO port selection register

9.3.1. IIC Address Register

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

Bit number	Bit symbol	Description
7~1	IICADD[7:1]	IIC address

9.3.2. IIC Transmit and Receive Data Register

IIC transmit and receive data register, used to control the working condition of communication.
IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

The specific application process is as follows:

In the send state, after the data is ballasted into the IICBUF, under the synchronous clock of the host. The data is sequentially shifted and sent out, the high position is in front. After 8 clocks, one byte is sent.

In the receive state, after the host's 8 clocks have passed, the data is written to the BUF. After the 9th clock, an interrupt is generated, telling the CPU to read the data in the IICBUF.

Writing data to IICBUF is conditional, when RD_SCL_EN=1, only IIC_RW=1, and SCLEN=0 can write data into IICBUF; Otherwise, the operation of writing IICBUF is prohibited. That is to say, if the condition is not satisfied, the operation of writing IICBUF cannot be successful, and the data cannot be written. IICBUF data will not change, but will also cause write confilicts.

For example: IICBUF already has been 55h. In case the condition of writing IICBUF is not satisfied, we want to write data 00h into IICBUF. The result is that the data in IICBUF is still 55h, and the write conflict flag IIC_WCOL is set to tell the user that the operation is abnormal.

When RD_SCL_EN=0, the data to be the slave is the value of the ballast IICBUFFER register when the interrupt signal is generated.

9.3.3. IIC Control Register

IICCON register, used to control the working condition of communication.

IICCON (E5H) IIC control register

Bit number	7	6	5	4
Symbol	-	-	IIC_RST	RD_SCL_EN
R/W	-	-	R/W	R/W
Reset value	-	-	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation, 0: IIC module works normally
4	RD_SCL_EN	The host reads the low clock line control bit 1: Enable the host to read and pull down the clock line function, 0: Disable the host read and pull down clock line function
3	WR_SCL_EN	The host writes the low clock line control bit, 1: Enable the function of writing and pulling down the clock line, 0: Disable the function of writing and pulling down the clock line
2	SCLEN	IIC clock enable bit: 1: Clock works normally, 0: Low the clock line
1	SR	IIC conversion rate control bit 1: The conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit: 1: IIC works normally, 0: IIC does not work

IICEN is module enable signal, when IICEN=1, the circuit works.

SR is the conversion rate control bit, SR=1 conversion ratecontrol off, port adapted to 100Kbps communication.

SCLEN is clock enable control bit, although the slave cannot generate the communication clock, the slave can extend the low time of the clock according to the protocol. SCLEN=0, clock line is locked at low level; SCLEN=1, release clock line. The premise of extending the low level of the clock is IICEN=1, otherwise the internal circuit will not have any effect on the IIC bus. SCLEN is often used to extend low time and make the host enter the wait state, so that the slave has enough time to process the data.

WR_SCL_EN is write low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

IIC_RW=0, according to the communication rate of the host and the time of processing the interrupt, it is determinded whether to lower the clock line, that is, configure the WR_SCL_EN bit.

When the CPU can process the interrupt and exit the interrupt within 8 IIC clocks. WR_SCL_EN=0 disable pull down the clock clock line function. At this time, the hardware will not automatically pull down the clock line when the interrupt arrives. When the CPU cannot process the interrupt and exit in the 8 IIC clocks, WR_SCL_EN=1 enables the clock line to be pulled down. At this point, the hardware automatically pulls down the clock line when the interrupt arrives, forcing the host to enter the wait state. When the data written to the IIC is read by the CPU, the software sets SCLEN.

RD_SCL_EN is read low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

RD_SCL_EN=1. when the slave receives the address byte or sends one byte and the host sends, SCLEN will be automatically pulled low by hardware, forcing the host to the enter the wait state. The release the IIC clock from the slave, the following two operations arerequired: first write the data to be sent to the IIC, set the software in IICBUF in SCLEN. The purpose of this design is to ensure that the data to be sent has been written in the IICBUF before the SCL is pulled high.

RD_SCL_EN=0, when the slave receives the address byte or sends one byte and the host sends an ACK, the slave immediately polls the data prepared in the IICBUFFER register to the transmit buffer register and then to the data line. Therefore, in order to ensure that data transmitted each time is correct, IICBUFFER prepares the next data to be sent in the interrupt service routine. The data received by the host is the last interrupted data, and the first time the data is received is ready for initialization.

Note: When you need to pull down the clock line, that is, WR_SCL_EN/RD_SCL_EN=1. Software should turn off the clock line until the last Byte data is sent and received. That is, WR_SCL_EN/RD_SCL_EN=0, the software should turn on the write low pull clock line before sending and receiving the last Byte data. This kind of operation can be self-regulated according to whether the host is software or hardware. The interrupt processing time is self-regulated.

IIC_RST is IIC module control enable bit, enable the IIC module reset function for 1 and disable the IIC module reset function when 0. Pay attention to configuration 1 reset IIC module all DFF triggers. The reset terminal of IIC_RST is global reset, and the other reset terminal are iic_rst_n. All iic_rst writes 0 first, then operate other register configurations..

9.3.4. IIC Status Register

IIC status register, used to reflect the status in the communication process and can be queried by the user.

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: Indicates that the start bit is detected; 0: Indicates that the start bit is not detected.
6	IIC_STOP	Stop signal flag 1: Indicates in the stop state; 0: Indicates that the stop bit is not detected.
5	IIC_RW	Read and write flag Record the read/write information obtained from the address byte after the last address match, 1: Indicates read operation; 0: Indicates write operation.
4	IIC_AD	Address data flag 1: Indicates that the most recently received or sent byte is data; 0: Indicates that the most recently received or sent byte is an address.
3	IIC_BF	IICBUF full flag bit: when receiving in IIC bus mode 1: Indicates that the reception is successful and the buffer is full; 0: Indicates that the reception is not completed and the buffer is still empty When sending in IIC bus mode: 1: Indicates that data transmission is in progress (not including the response bit and stop bit), and the buffer is still full;

		0: Indicates that the data transmission has been completed (not including the response bit and stop bit), and the buffer is empty.
2	IIC_ACK	Reply flag 1: Indicates an invalid response signal; 0: Indicates an effective response signal.
1	IIC_WCOL	Write conflict flag 1: Indicates that when the IIC is sending the current data, new data is trying to be written into the sending buffer; the new data cannot be written into the buffer; 0: No write conflict occurred.
0	IIC_RECOV	Receive overflow flag 1: Indicates that new data is received when the previous data received by IIC has not been taken away, and the new data cannot be received by the buffer; 0: Indicates that no receive overflow has occurred.

IIC_START: Start signal status bit, IIC_START is set when the start signal is detected, Indicating that the bus is busy.

IIC_STOP: Stop signal status bit, IIC_START is set when the start signal is detected, indicating that the bus is idle. When the start signal is detected, the hardware is cleared, indicating that communication begins.

IIC_AD: Address data flag. It indicates whether the byte currently received or sent is an address or data. IIC_AD =0, flag is currently received or sent byte is the address; IIC_AD = 1 flag is currently received or sent byte is the data; Start signal, stop signal, non-response signal have no effect on this status bit. This status bit change occurs on the falling edge of the 8h clock.

IIC_RW: Read and write flag. The flag bit is recorded the read and write information bits obtained from the address is matched. IIC_RW = 1 means the host reads the slave. RW = 0 means the host writes the slave. Start signal, stop signal, non-answer signal (NACK) is cleared IIC_RW. This status bit change occurs on the falling edge of the 8h clock.

IIC_BF: BUFFER full flag. It indicates that the transceiver buffer is currently full or empty. IIC_BF=0 indicates that the buffer does not receive data and the buffer is empty; IIC_BF=1 indicates that the buffer receive data and the buffer is full. This status bit can only be set and cleared indirectly, not directly.

Address matching and IIC_RW=0, IIC_BF will be set after the falling edge of the 8h clock, indicating that the IICBUF has received the data. The IICBUF should be read during the execution of the interrupt routine, and the read IICBUF will indirectly clear the BF flag. If the host does not read IICBUF and the host continues to send data, a receive overflow will occur. Although the slave still receives the host to send data and is ballasted to the IICBUF. But NACK signals are still sent, giving an invalid reply.

Address matching and IIC_RW=1. after the slave receives the Address byte, the IIC_BF flag will not be set; IIC_RW=1 indicates the operation of the master to read the slave, the slave operation needs to write data to the IICBUF, and the slave writes IICBUF operation to set the IICBUF. The software then sets SCLEN to release the clock line; The host sends the synchronous clock. After the 8th clock is passed, the IICBUF is cleared by hardware after the data in the IICBUF is sent out.

IIC_ACK: Answer flag. Regardless of whether the host is a read or write operation, the slave samples the data line from the rising edge of the ninth clock and records the response information. The acknowledge bits are divided into a valid acknowledgment ACK and a non-valid acknowledgement bit NACK. That is to say, the rising edge of the ninth clock samples the data to 0, indicating that the ACK is valid, and the IIC_ACK is cleared. If data 1 is sampled, NACK is set, indicating non-response. After the non-acknowledgment signal, the host will send a stop signal to announce the end of the communication. The start signal will clear this status bit.

IIC_WCOL: Write conflict flag. IICBUF only when IIC_RW=1. RD_SCL_EN=1 and SCLEN=0 can be written by the CPU. Any other attempt to write to IICBUF is forbidden. If the above conditions are not met, the write IICBUF operation occurs. Then the data will not be written to IICBUF, and the conflict flag IIC_WCOL will be set. This flag needs to be cleared by software.

IIC_RECOV: Receive overflow flag.In the case of IICBUF full, that is, in the case of data in the IICBUF. If IIC received new data, it will receive overflow and IIC RECOV will set.At the same time, the data in the IICBUF will not be updated, and the newly received data will be lost. This status bit also requires software to clear, otherwise it will affect the subsequent communication. This kind of situation will only appear in IICRW=0. BF=1. And the CPU will appear when it does not read IICBUF.

9.3.5. IIC Transmit and Receive Data Buffer Register

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUFFER	IIC transmit and receive data buffer register; when RD_SCL_EN is 0, when the master reads data, the data in IICBUFFER will be sent to the slave send buffer register 2 clocks after the interrupt, as the data sent by the slave. So prepare IICBUFFER interrupt data before interrupt generation.

9.3.6. IIC Function Control Register

PERIPH_IO_SEL (F2H) IIC/INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	-	-
R/W	-	R/W	R/W	-	-
Reset value	-	1	0	-	-
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
6	IIC_AFIL_SEL	IIC port analog filter selection enable 1: Select the analog filter function; 0: Not Select the analog filter function
5	IIC_DFIL_SEL	IIC port digital filter selection enable 1: Select the digital filter function; 0: Not Select the digital filter function

9.3.7. IIC Interrupt Related Registers

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	EX3	IIC interrupt enable 1: Interrupt enabled; 0: Interrupt disabled;

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	IE3	IIC interrupt flag

		1: With interrupt flag 0: No interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	IPL1.3	IIC interrupt priority 0: Low priority; 1: High priority

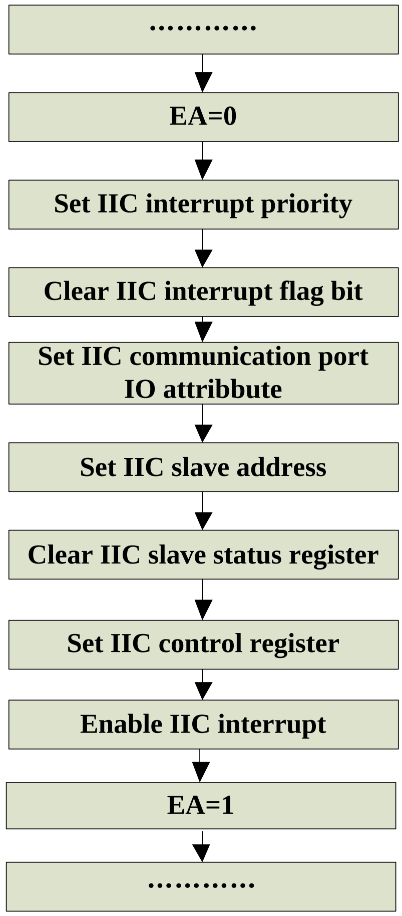
9.3.8. Secondary Bus Registers

IIC_IO_SEL (2CH) IIC mapping IO port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	IIC_IO_SEL[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	IIC_IO_SEL[1:0]	IIC port selection enable 00: PA0/PA1 port select IIC function 01: PB5/PC0 port select IIC function 10: PA1/PD6 port select IIC function 11: Reserved When PB5/PC0 is used as an IIC port, there is no SR control function, and the automatic logic control changes to open leakage output. When PB5/PC0 is GPIO, there is no open leakage output function

9.4. IIC Configuration Process



IIC configuration flow chart

Note: The IIC bus pull-up resistor is 4.7k~10k, and the filter capacitor to the ground is recommended to be 10pF~100pF close to the pin chip.

10. UART

There are 2 UART modules in the BF7612DMXX-SJLX series, UART0 supports 6-way IO port mapping, UART1 supports 2-way IO port mapping, and can only correspond to one set of mappings at the same time. UART module interface features:

- Support full-duplex, half-duplex serial
- Independent dual buffer receiver and single buffer transmitter
- Programmed baud rate (10bit analog-to digital divider)
- Interrupt-driven or polling operation:
  - transmit completed
  - receive full
  - receive overflow, parity error, frame error
- Support hardware parity production and check
- Programmable 8bit or 9bit character length
- STOP bit 1 or 2 can be selected
- Support multiprocessor mode
- Support TXD/RXD pin position exchange
- Support TXD/RXD independent enable

10.1. UART Function Description

10.1.1. Baud Rate Generation

Baud rate generation modulo Baud_Mod = {UART0_BDH[1:0], UART0_BDL}.

Baud rate calculation formula: When Baud_Mod=0, the baud rate clock is not generated. When Baud_Mod=1~1023. UART0 baud rate = BUSCLK/(16xBaud_Mod).

BUSCLK uses the frequency division clock of System clock source and is fixed at 24MHz. Each time the baud rate register is configured, the internal counter will be cleared to regenerate the baud rate signal. Communication requires that the transmitter and receiver use the same baud rate. The allowable baud rate deviation range for communication: 8/(11*16)=4.5%.

10.1.2. Transmitter Function

Transmit data flow: Trammitted by writing UART_BUF data, sending stop bit after sending stop bit. Software clear interrupt flag and waits for the next write. The transmitter output pin (TXD) idle state defaults to a logic high state. The entire transmission process must be performed when the module is enabled. By writing data into the data register (UART_BUF), the data will be directly saved to the transmitting data buffer and the transmitting process will be started. In the subsequent complete sending process, the data buffer is locked, and the configuration write data register is invalid until the sending is completed after the stop bit, write UART_BUF again to restart a new transmission.

The central element of the serial port transmitter is the transmit shift register with a length of 10/11/12 bits (depending on the setting in the DATA_MODE control bit). Assuming DATA_MODE=0, select the normal 8-bit data mode. In 8-bit data mode, there are 1 start bit, 8 data bits, and 1/2 stop bits in the shift register. Both transmitting and receiving are in little-endian mode (LSB first). When the transmitter is not enabled, the TXD port is released, and the corresponding PAD can be used as other functions.

10.1.3. Receiver Function

The receiver is enabled by setting the receive enable bit in UART_CON1. Of course, the entire receiving process must be performed when the module is enabled.

Receiving data flow: When the receiving enable is valid, the data is received at any time, the receiving interrupt is set after receiving the stop bit, and the software clears the interrupt flag.

The currently received data will have a detection mechanism, which can detect three types of errors: receiving overflow, frame error, and parity error, all of which require software to clear the flag. It is recommended that after detecting the receiving interrupt, read the status flag, read the data buf, and finally clear the received data status flag.

The data character is composed of a logic 0 start bit, 8 (or 9) data bits (LSB first) and a logic 1 stop bit (1bit). After receiving the stop bit into the receiving shifter, if the receiving data register is not full(RI0/1=0), the data character is transferred to the receiving data register, and the receiving data register is full status flag is set(RI0/1=1). If RI0/1 whose receive data register is full has been set at this time, the overflow (UART0/1_R) status flag is set, and new data will be lost. Because the receiver is double-buffered, the program has a full character time for R to fetch after setting RI0/1 and before R fetches the data in the receive data buffer to avoid receiver overflow. When the program detects that the receive data register is full (RI0/1=1), it gets data from the receive data register through RUART0/1_BUF.

10.1.4. Receiver Sample Method

The receiver uses a 16 times baud rate clock for sampling. The receiver searches for the falling edge on the RXD serial data input pin by extracting logic level samples at 16 times the baud rate. The falling edge is defined as logic 0 samples after 3 consecutive logic 1 samples. The 16 times baud rate clock is used to divide the bit time into 16 segments, which are labeled RT1 to RT16.

The receiver then samples each bit time of RT8, RT9 and RT10, including the start bit and stop bit, to determine the logic level of the bit. The logic level is the logic level of the vast majority of samples taken during the bit time. When the falling edge is positioned, the logic level is 0 to ensure that this is the real start bit, not noise. If at least two of these three samples are 0, the receiver assumes that it is synchronized with the receiver character and starts shift receives the following data, if the above conditions are not met, exit the state machine and return to the state of waiting for the falling edge. The falling edge detection logic keeps looking for a falling edge. If an edge is detected, the sample clock resynchronizes the bit time.

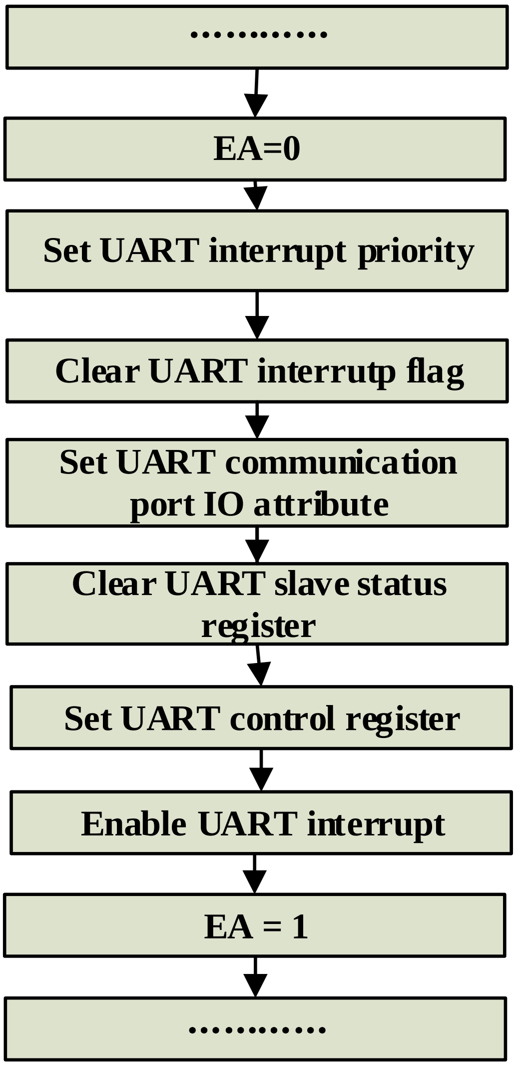
10.1.5. Multiprocessor Mode

In multi-processor mode, it only works in 9-bit mode. When the received UART0/1_R8 bit=1. The receive interrupt is set, otherwise it is not set. The function of this mechanism is to use hardware detection to eliminate the software overhead of processing unimportant information characters. Allow receivers to ignore characters in messages used for different receivers.

In this application system, all receivers estimate the address character (bit 9 = 1) of each message. Once it is determined that the information is intended for different receivers, subsequent data characters (bit 9 = 0) will not be received.

Configuration process: Configure receiving enable, configure multiprocessor mode, receive Address data (the 9th bit = 1), receive and generate an interrupt, the application confirms whether the Address matches, if it matches, the configuration closes the multiprocessor mode, and all subsequent data (The 9th bit = 0) can be received and interrupted, until the next Address data is received, the Address does not match, then the multi-processor mode is turned on, then all subsequent data will not be received, until the next Address data, in turn, loop application.

10.2. UART Configure Process



UART initial configure process

Recommended application process:

1. Configuration module enable, receive enable, mode select: UART_CON1;
2. Configure baudrate, open interrupt enable: UART_BDL, UART_CON2;
3. Write UART_BUF to start transmitting data. After detecting the transmitting interrupt, clear the interrupt flag tx_empty_if;
4. When the receiving interrupt is detected, first read the receiving status UART0/1_STATE, then read UART0/1_R8 and UART0/1_BUF, and finally clear the receiving status flag (UART0/1_STAT[3:0] = 0), Once the receiving process is completed, wait for the next receiving interrupt.

5. If the configuration interrupt is not enabled and the program executes the UART function, it also needs to read the status flag first, then read UART0/1_R8 and UART0/1_BUF, and finally clear the status flag.
6. Interrupt flag bit clearing operation. In full-duplex operation, the clear flag bit operation requires writing 0 for the effective interrupt bit and writing 1 for other interrupt bits (writing 1 is an invalid operation), otherwise it is easy to misuse. For example: when the transmission interrupt is valid, you need to write UART0_STATE = 0x0F; (that is, configure UART0_STATE [0:3] = 0x0F, and write UART0/1_R8 is invalid. When UART0/1_T8 is in 9-bit mode and no parity, you need to configure valid transmission data).
7. 8-bit mode: the parity check is disabled.
   9-bit mode: When the parity bit is enabled, when the ninth bit is not enabled, the ninth bit is UART0/1_T8 written in. There are only transmitting and receiving interrupts. The error flag only marks the error detection of the current data, and only the corresponding bit is cleared by writing 0. There is no error interrupt. The transmitting interrupt is set to 1 after the stop bit is sent, and the software is cleared to 0. The receiving interrupt is receiving Set to 1 after the stop bit is completed, cleared by software.

   Multi-processor mode: only work in 9-bit mode, when the received UART0_R8 bit = 1, the receive interrupt is set, otherwise it is not set. When using the multi-processor mode, configure the receive enable, configure the multi-processor mode, receive the address data (the 9th bit = 1), receive and generate an interrupt, the application confirms whether the address matches, and the configuration closes the multi-processor mode if it matches. Data (the 9th bit = 0) can be interrupted by the receive interrupt until the next address data is received. If the address does not match, the multi-processor mode is turned on, and all subsequent data will not be received until the next address data is cycled in turn application.

   Hardware response: Transmit data, start by writing UART0/1_BUF value, set the transmitting interrupt flag after transmitting the stop bit, and clear the interrupt flag by software, and wait for the next write. When the receiving data is enabled, the data can be received at any time. After receiving the stop bit, the receiving interrupt is set and the software clears the interrupt flag. The currently received data will have a detection mechanism, which can detect three types of errors: receiving overflow, frame error, and parity error, all of which require software to clear the flag. It is recommended that after detecting the receiving interrupt, read the status flag and clear all the receiving status flags UART0/1_STATE [0:3].
   Note: Mapping synchronous output functions is not supported.

10.3. UART Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xBD	UART0_BDL	RW	0000_0000b	UART0 baud rate control register
0xBE	UART0_CON1	RW	x000_0000b	UART0 control register1
0xBF	UART0_CON2	RW	xxxx_1100b	UART0 control register2
0xC0	UART0_STATE	R/RW	x000_0000b	UART0 status flag register
0xC1	UART0_BUF	RW	1111_1111b	UART0 data register
0xC2	UART_IO_CTRL	RW	xxxx_xx00b	UART pin exchange control register
0xC3	UART_IO_CTRL1	RW	xxxx_0000b	UART pin enable control register
0xC5	UART1_BDL	RW	0000_0000b	UART1 baud rate control register
0xC6	UART1_CON1	RW	x000_0000b	UART1 control register1
0xC7	UART1_CON2	RW	xxxx_1100b	UART1 control register2
0xC8	UART1_STATE	R/RW	x000_0000b	UART1 status flag register
0xC9	UART1_BUF	RW	1111_1111b	UART1 data register
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2

UART register list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x2B	UART_IO_SEL	RW	xxxx_0000b	UART mapping IO port selection register

10.3.1. UART0 Baud Rate Control Register

UART0_BDL (BDH) UART0 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register Baud rate modulus divisor register, low 8 bits, Baud_Mod = {UART0_BDH[1:0], UART0_BDL}, When Baud_Mod = 0, no baud rate clock is generated, When Baud_Mod = 1~1023. Baud rate = BUSCLK/(16xBaud_Mod)

10.3.2. UART0 Control Register1

UART0_CON1 (BEH) UART0 control register1

Bit number	7	6	5	4
Symbol	-	UART0_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_ENABLE	Module enable, 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable, 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi- processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection, 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

10.3.3. UART0 Control Register 2

UART0_CON2 (BFH) UART0 control register2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	-	-	R/W	R/W	R/W	
Reset value	-	-	-	-	1	1	0	0

Bit number	Bit symbol	Description
3	TX_EMPTY_IE	Transmit interrupt enable 1: Interrupt enable, 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable, 0: Interrupt disable (used in polling mode)
1~0	UART0_BDH	The upper 2 bits of the baud rate modulus divisor register

10.3.4. UART0 Status Flag Register

UART0_STATE (C0H) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/RW	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_R	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	The 9th data of the receiver, read only
5	UART0_T8	The 9th data of the transmitter, read only when parity check is enabled
4	TI0	Transmit interrupt flag: 1: Transmit buffer is empty 0: Transmit buffer is full, software write 0 to clear, write 1 is invalid
3	RI0	Receive interrupt flag: 1: Receive buffer is full 0: Receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	UART0_R	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	UART0_F	Frame error flag: 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	UART0_P	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

10.3.5. UART0 Data Register

UART0_BUF (C1H) UART0 data register

Bit number	7	6	5	4	3	2	1	0

Symbol	-
R/W	R/W
Reset value	FF

Bit number	Bit symbol	Description
7~0	--	Data register Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

10.3.6. UART Pin Exchange Control Register

UART_IO_CTRL (C2H) UART pin exchange control register

Bit number	7~2	1	0
Symbol	-	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	-	R/W	R/W
Reset value	-	0	0

Bit number	Bit symbol	Description
7~2	--	Reserved
1	UART1_PAD_CHANGE	UART1 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange
0	UART0_PAD_CHANGE	UART0 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange

10.3.7. UART Pin Enable Control Register

UART_IO_CTRL1 (C3H) UART pin enable control register

Bit number	7~4	3	2	1	0
Symbol	-	UART1_RXD_DIASB	UART1_TXD_DIASB	UART0_RXD_DIASB	UART0_TXD_DIASB
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	UART1_RXD_DIASB	UART1 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled

2	UART1_TXD_DIASB	UART1 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled
1	UART0_RXD_DIASB	UART0 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
0	UART0_TXD_DIASB	UART0 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled

10.3.8. UART1 Baud Rate Control Register

UART1_BDL (C5H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register Baud rate modulus divisor register, low 8 bits, Baud_Mod={UART1_BDH[1:0], UART1_BDL}, When Baud_Mod=0, no baud rate clock is generated, When Baud_Mod=1~1023. Baud rate = BUSCLK/(16xBaud_Mod)

10.3.9. UART1 Control Register1

UART1_CON1 (C6H) UART1 control register1

Bit number	7	6	5	4
Symbol	-	UART1_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description

7	--	Reserved
6	UART1_ENABLE	Module enable, 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable, 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi- processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection, 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

10.3.10. UART1 Control Register 2

UART1_CON2 (C7H) UART1 control register2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	-	-	-	-	R/W	R/W	R/W	
Reset value	-	-	-	-	1	1	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	TX_EMPTY_IE	Transmit interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register, high 2 bits

10.3.11. UART1 Status Flag Register

UART1_STATE (C8H) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	R8	T8	TX_EMPTY_IF
R/W	-	R	R/RW	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	FRX_FULL_I	RX_OVERFLOW_IF	FRAME_ERR_IF	PARITY_ERR_IF

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	R8	The 9th data of the receiver, read only
5	T8	The 9th data of the transmitter, read only when parity check is enabled
4	TX_EMPTY_IF	Transmit interrupt flag: 1: Transmit buffer is empty 0: Transmit buffer is full, software write 0 to clear, write 1 is invalid
3	FRX_FULL_I	Receive interrupt flag: 1: Receive buffer is full 0: Receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	RX_OVERFLOW_IF	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	FRAME_ERR_IF	Frame error flag 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	PARITY_ERR_IF	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

10.3.12. UART1 Data Register

UART1_BUF (C9H) UART1 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	-	UART1 data register Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

10.3.13 Interrupt Registers

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
2	IE10	UART1 interrupt flag 1: With interrupt flag 0: No interrupt flag
1	IE9	UART0 interrupt flag 1: With interrupt flag 0: No interrupt flag

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
2	EX10	UART1 interrupt enable 1: Interrupt enable; 0: Interrupt disable;
1	EX9	UART0 interrupt enable 1: Interrupt enable; 0: Interrupt disable;

10.3.14. UART Mapping IO Port Selection Register

UART_IO_SEL (2BH) UART mapping IO port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	UART1_IO_SEL	UART0_IO_SEL		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	UART1_IO_SEL	UART1 port selection enable 0: PB1/2(RXD1_A/TXD1_A) port select UART1 function 1: PB6/7(RXD1_B/TXD1_B) port select UART1 function
2~0	UART0_IO_SEL	UART0 port selection enable 000: PA0/1(RXD0_A/TXD0_A) port select UART0

		function 001: PB3/4(RXD0_B/TXD0_B) port select UART0 function 01x: PC0/1(RXD0_D/TXD0_D) port select UART0 function 100: PD6/PA1(RXD0_E/TXD0_E) port select UART0 function 101: PD7/PA0(RXD0_F/TXD0_F) port select UART0 function 11x: PD4/5(RXD0_C/TXD0_C) port select UART0 function

11. PWM

11.1. PWM0

11.1.1. PWM0 Features

- The clock source is pwm_clk: 24MHz;
- 16-bit counter;
- Pulse width = (PWM0_CHx_CNT)
- Cycle = (PWM0_MOD+1)
- Duty cycle = pulse width/period
- Support up to 4 channels, select PWM0_A/B/C/D or PWM0_A1/B1/C1/D1
  - The period is the same
  - Each channel is individually enabled
  - The polarity of each channel can be configured
  - The duty cycle of each channel can be configured, and the duty cycle of PWM0_B/C/D (PWM0_B1/C1/D1) can be selected as PWM0_A (PWM0_A1) configuration, you can also choose to configure the duty cycle of its own channel

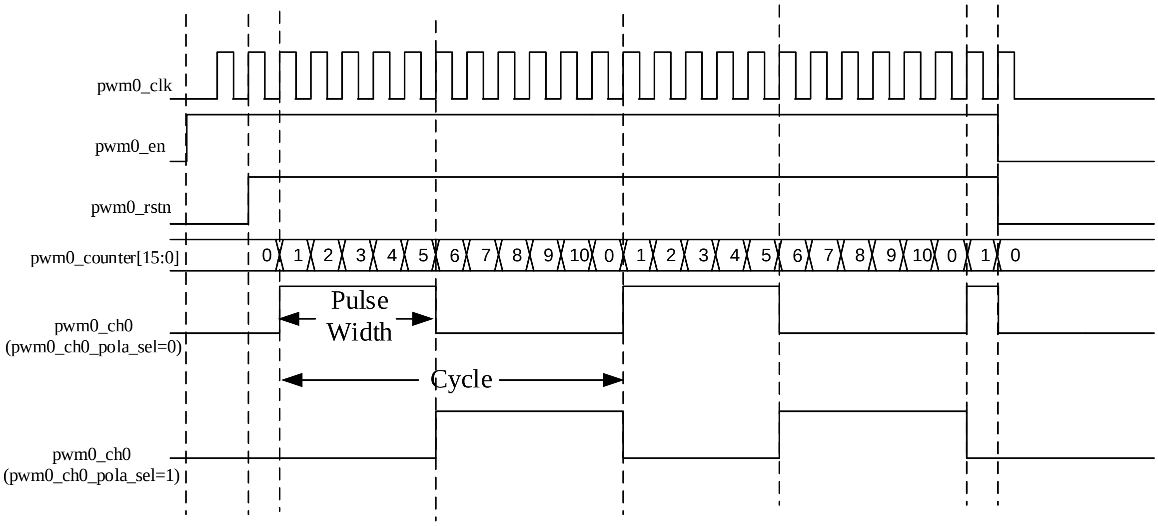
11.1.2. Function Description

The PWM0 pulse width modulation module can be configured through registers for both period and pulse width, but the configuration of the registers must be enabled when PWM0 is enabled (active high), and each group of registers (including PWM0_MOD_L/H, PWM0_CHX_CNT_L/H) must be configured in order from low to high, in order to ensure the correct counting of the internal counter of PWM0Module and avoid generating wrong waveforms. These configuration values update the register value by waiting until the counter changes from (PWM0_MOD) to (PWM0_MOD+1), that is, after a full cycle, the period and duty cycle are updated.

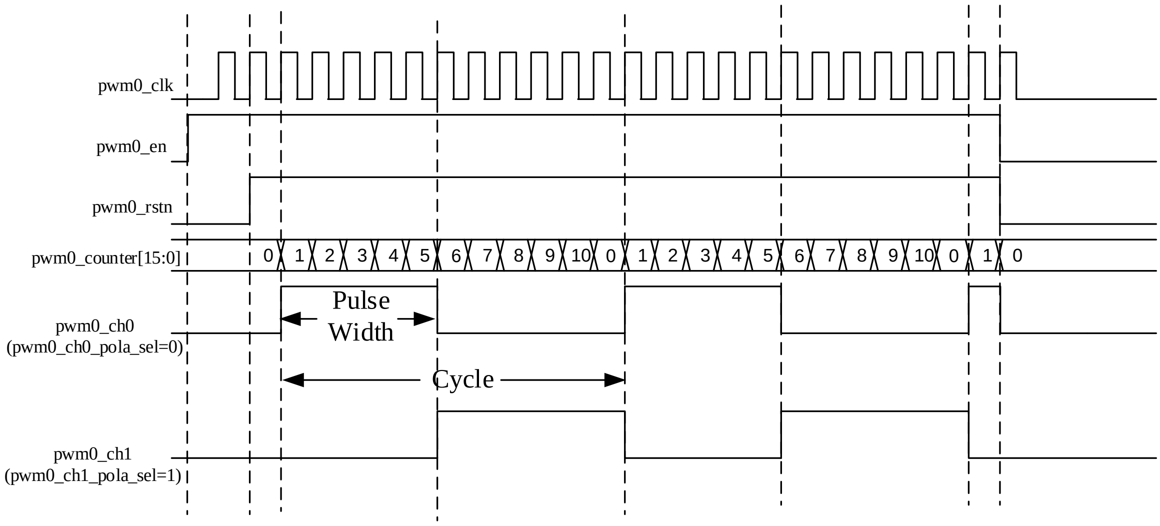
PWM0 module supports 4 channels, each channel can be individually controlled and enabled, sharing a 16-bit counter, the counting clock is 24MHz and System clock is synchronized. The period of the PWM0 signal is determined by the value of the period configuration register (PWM0_MOD), the duty cycle is determined by the setting in the channel register (PWM0_CHn_CNT), and the polarity of the PWM0 signal is determined by the setting in the PWM0_CH_CTRL control bit. 0% and 100% duty cycle is configurable

The PWM0 counter starts to count up from 0x0000, and the output flips when PWM0_CHn_CNT is counted. This period is the pulse width, and it continues to count until the count overflows when PWM0_MOD+1 is counted. If PWM0_CH0_POLA_SEL=0, the PWM0 signal enters the low state when the output is inverted, and the PWM0 signal enters the high state when the count overflows. If PWM0_CH0_POLA_SEL=1, the PWM0 signal enters a high state when the output is inverted, and the PWM0 signal enters a low state when the count overflows.

When the channel count register (PWM0_CHn_CNT) is set to 0x0000, the duty cycle is 0%; when the channel count register (PWM0_CHn_CNT) is set to a value greater than the value set by the period configuration register (PWM0_MOD), a 100% duty cycle can be achieved. The counter is automatically reloaded and will not stop by itself. It will not stop until the register PWM0 is enabled and turned off, and the counter is cleared.



(PWM0_CH0_CNT=5, PWM0_MOD=10, duty_cycle=5/11)



(PWM0_CH0, PWM0_CH1 complementary output)

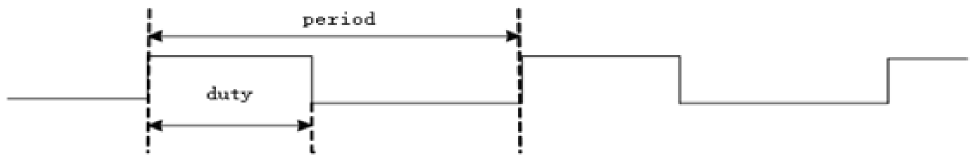
11.2. PWM1/2

11.2.1. PWM1/2 Features

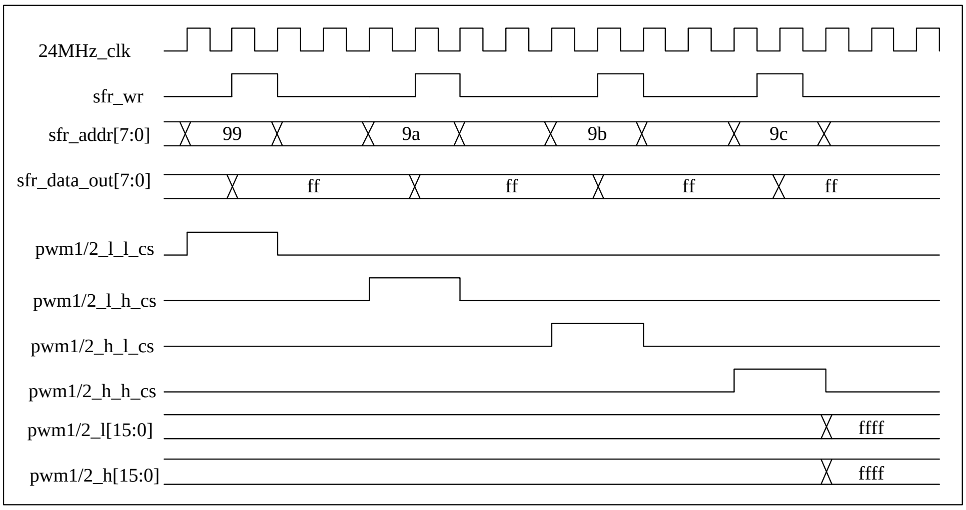
- Clock source: pwm_clk: 24MHz
- PWM1/2 high level control register and low level control register both are 16-bit registers
- Output period: $T_{PWM1/2\_data}$ = (PWM1/2_H + PWM1/2_L)* Tpwm_clk (μs)
- Output duty: $D_{PWM1/2\_data}$ = PWM1/2_H/(PWM1/2_L + PWM1/2_H)
- PWM1 supports 1 channel output, selects the output channel through PWM_IO_SEL.1
- PWM2 supports 1 channel output, selects the output channel through PWM_IO_SEL.2

11.2.2. Function Description

PWM1/2 waveform intent



PWM1/2 PWM module can be configured through registers for both high and low level time, but the configuration of registers must be enabled when PWM1/2 is enabled (active high), and the high level control register and low level control register must be configured in order from low to high, in order to ensure the correct counting of the internal counter of PWM1/2Module to avoid generating wrong waveforms. These configuration values update the period and duty cycle after a full cycle.



PWM1/2 timing diagram

11.3. PWM Port Configuration

Before using the PWM module, you need to configure the corresponding port as a PWM channel. The BF7612DMXX-SJLX provides PWM_IO_SEL register, configure Bit0 of this register to control PWM0 output channel, configure Bit1 of this register to control PWM1 output channel, configure Bit2 of this register to control PWM2 output channel.

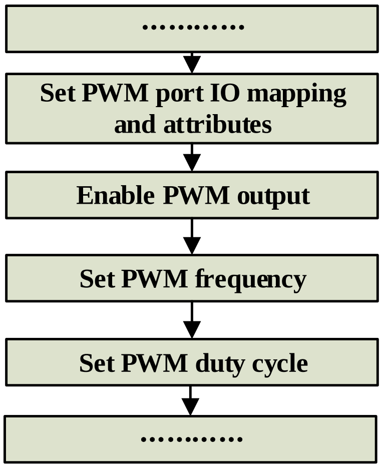
Secondary bus register:

PWM_IO_SEL (28H) PWM select enable register

Bit number	7~3	2	1	0
Symbol	-	PWM2_IO_SEL	PWM1_IO_SEL	PWM0_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	PWM2_IO_SEL	PWM2 port select enable 0: PD1 port selects PWM2_A function 1: PC7 port selects PWM2_A1 function
1	PWM1_IO_SEL	PWM1 port select enable 0: PD0 port selects PWM1_A function 1: PC6 port selects PWM1_A1 function
0	PWM0_IO_SEL	PWM0 port select enable 0: PB0/1/2/3 port select PWM0_A/B/C/D function 1: PB5/PC0/PC3/PC5 port select PWM0_A1/B1/C1/D1 function

11.4. PWM0 Configuration Process



PWM0 Schematic diagram of configuration process

PWM0 register configuration description process:

1. Configure PWM0 control register PWM0_CH_CTRL (channel enable and polarity selection);
2. Configure the enable register PWM0_EN, configure the count register PWM0_CHx_CNT_L/H, and the period register PWM0_MOD_L/H (last configuration) to start working.

Note:

1. The period and duty cycle registers need to be configured with PWM0_EN=1. The count register and period register are allowed to be configured during the working process, and multiple channels are allowed to be updated at the same time in the same cycle, and PWM0_CH_CTRL is not allowed to be configured during the update cycle. Only PWM0_EN=0 can change the PWM0_CH_CTRL configuration. When PWM0_EN=1, writing count register and period configuration register will directly update the duty cycle and period. During the operation of the counter, the write count register and the period configuration register will be latched, and the register value will be updated when the counter (PWM0_MOD) becomes (PWM0_MOD+1), that is, the duty cycle and period will be updated after a complete period.
2. Frequency range: 370Hz ~ 369kHz recommended.

11.5. PWM Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x99	PWM1_L_L	RW	0000_0000b	PWM1 low level control register (low 8 bits)
0x9A	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8 bits)
0x9B	PWM1_H_L	RW	0000_0000b	PWM1 high level control register (low 8 bits)
0x9C	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8 bits)
0x9D	PWM2_L_L	RW	0000_0000b	PWM2 low level control register (low 8 bits)
0x9E	PWM2_L_H	RW	0000_0000b	PWM2 low level control register (high 8 bits)
0x9F	PWM2_H_L	RW	0000_0000b	PWM2 high level control register (low 8 bits)
0xA1	PWM2_H_H	RW	0000_0000b	PWM2 high level control register (high 8 bits)
0xA2	PWM_EN	RW	xxx0_0000b	PWM control register
0xA3	PWM0_CH_CTRL	RW	0000_0000b	PWM0 control register
0xA4	PWM0_CH0_CNT_L	RW	0000_0000b	PWM0 channel 0 count value configuration register low 8 bits
0xA5	PWM0_CH0_CNT_H	RW	0000_0000b	PWM0 channel 0 count value configuration register high 8 bits
0xA6	PWM0_CH1_CNT_L	RW	0000_0000b	PWM0 channel 1 count value configuration register low 8 bits
0xA7	PWM0_CH1_CNT_H	RW	0000_0000b	PWM0 channel 1 count value configuration register high 8 bits
0xA9	PWM0_CH2_CNT_L	RW	0000_0000b	PWM0 channel 2 count value configuration register low 8 bits
0xAA	PWM0_CH2_CNT_H	RW	0000_0000b	PWM0 channel 2 count value configuration register high 8 bits
0xAB	PWM0_CH3_CNT_L	RW	0000_0000b	PWM0 channel 3 count value configuration register low 8 bits
0xAC	PWM0_CH3_CNT_H	RW	0000_0000b	PWM0 channel 3 count value configuration register high 8 bits
0xAD	PWM0_MOD_L	RW	0000_0000b	PWM0 period configuration register low 8 bits

0xAE	PWM0_MOD_H	RW	0000_0000b	PWM0 period configuration register high 8 bits

PWM register list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x28	PWM_IO_SEL	RW	xxxx_x000b	PWM select enable register

11.5.1. PWM1 Low Level Control Registers

PWM1_L_L (99H) PWM1 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_L [7:0]							
R/W	R/W							
Reset value	0							

PWM1_L_H (9AH) PWM1 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_H [7:0]							
R/W	R/W							
Reset value	0							

11.5.2. PWM1 High Level Control Registers

PWM1_H_L (9BH) PWM1 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_L [7:0]							
R/W	R/W							
Reset value	0							

PWM1_H_H (9CH) PWM1 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H [7:0]							
R/W	R/W							
Reset value	0							

11.5.3. PWM2 Low Level Control Registers

PWM2_L_L (9DH) PWM2 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_L [7:0]							

R/W	R/W
Reset value	0

PWM2_L_H (9EH) PWM2 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_H [7:0]							
R/W	R/W							
Reset value	0							

11.5.4. PWM2 High Level Control Registers

PWM2_H_L (9FH) PWM2 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_L [7:0]							
R/W	R/W							
Reset value	0							

PWM2_H_H (A1H) PWM2 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_H [7:0]							
R/W	R/W							
Reset value	0							

11.5.5. PWM Control Register

PWM_EN (A2H) PWM control register

Bit number	7	6	5	4
Symbol	-	-	PWM0_CH3_CMOD	PWM0_CH2_CMOD
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH1_CMOD	PWM2_EN	PWM1_EN	PWM0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5~3	PWM0_CHn_CMOD (n=3~1)	PWM0 channel n duty cycle mode select bit 1: Select PWM0_A (PWM0_A1) duty cycle; 0: Select own channel duty cycle Channel 1: PWM0_B (PWM0_B1) Channel 2: PWM0_C (PWM0_C1)

		Channel 3: PWM0_D (PWM0_D1)
2	PWM2_EN	PWM2 module enable register 1: Enable; 0: Disable
1	PWM1_EN	PWM1 module enable register 1: Enable; 0: Disable
0	PWM0_EN	PWM0 module enable register 1: Enable; 0: Disable

11.5.6. PWM0 Control Register

PWM0_CH_CTRL (A3H) PWM0 control register

Bit number	7	6	5	4
Symbol	PWM0_CH3_ POLA_SEL	PWM0_CH2_ POLA_SEL	PWM0_CH1_ POLA_SEL	PWM0_CH0_ POLA_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH3_EN	PWM0_CH2_EN	PWM0_CH1_EN	PWM0_CH0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~4	PWM0_CHn_POLA_SEL (n=3~0)	Channel n polarity selection 1: The count value overflow makes the output low; 0: The count value overflow makes the output high; Channel 0: PWM0_A (PWM0_A1) Channel 1: PWM0_B (PWM0_B1) Channel 2: PWM0_C (PWM0_C1) Channel 3: PWM0_D (PWM0_D1)
3~0	PWM0_CHn_EN (n=3~0)	Channel n enable bit 1: Enable; 0: Disable

11.5.7. PWM0 Channel Count Value Configuration Registers

The following registers: configure the duty cycle of the PWM0 output channels
Channel 0: PWM0_A (PWM0_A1), Channel 1:PWM0_B (PWM0_B1)
Channel 2: PWM0_C (PWM0_C1), Channel 3: PWM0_D (PWM0_D1)

PWM0_CH0_CNT_L (A4H) PWM0 channel 0 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH0_CNT_H (A5H) PWM0 channel 0 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH1_CNT_L (A6H) PWM0 channel 1 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH1_CNT_H (A7H) PWM0 channel 1 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH2_CNT_L (A9H) PWM0 channel 2 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH2_CNT_H (AAH) PWM0 channel 2 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_H[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH3_CNT_L (ABH) PWM0 channel 3 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_L[7:0]							
R/W	R/W							
Reset value	0							

PWM0_CH3_CNT_H (ACH) PWM0 channel 3 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_H[7:0]							
R/W	R/W							

Reset value	0

11.5.8. PWM0 Period Configuration Registers

PWM0_MOD_L (ADH) PWM0 period configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_L[7:0]	PWM0 count period configuration register low 8 bits Configure the PWM output period

PWM0_MOD_H (AEH) PWM0 period configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_H[7:0]	PWM0 count period configuration register high 8 bits Configure the PWM output period

12. Touch Key

12.1. Features

Features of CSD:

- Three modes of CSD charge and discharge clock are available
  - Fixed frequency division of system clock 6M~369K
  - PRS 1.5M normal distribution
  - PRS 1.5M uniform distribution
- CSD count clock 24M, 12M, 6M, 4M optional
- The counting bit width is 9~16 bits optional
- Only support asynchronous scan mode

12.2. Function Description

The BF7612DMXX-SJLX realizes the application of multiple functions through a series of registers. The relationship between the capacitance detection related quantity and the SFR value is as follows：

The count value is proportional to RESO, Rb resistance, PULL_I_SELA_H, and inversely proportional to VTH_SEL. Under the condition of ensuring complete charge and discharge, it is proportional to the charge and discharge frequency set by PRS_DIV.

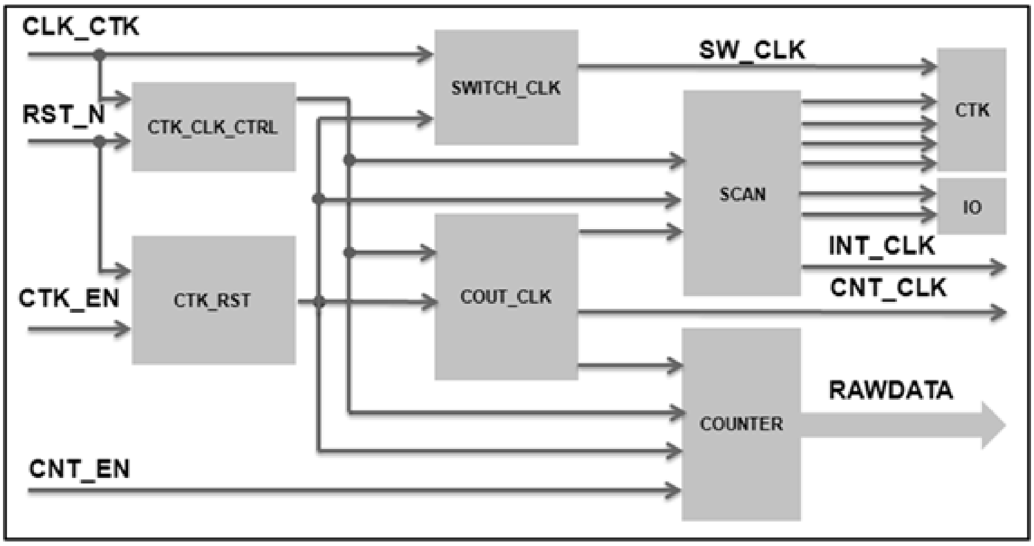
The channel touch change is proportional to RESO and Rb, and inversely proportional to VTH_SEL. Under the condition of ensuring complete charge and discharge, it is proportional to the charge and discharge frequency set by PRS_DIV and the amount of touch change.

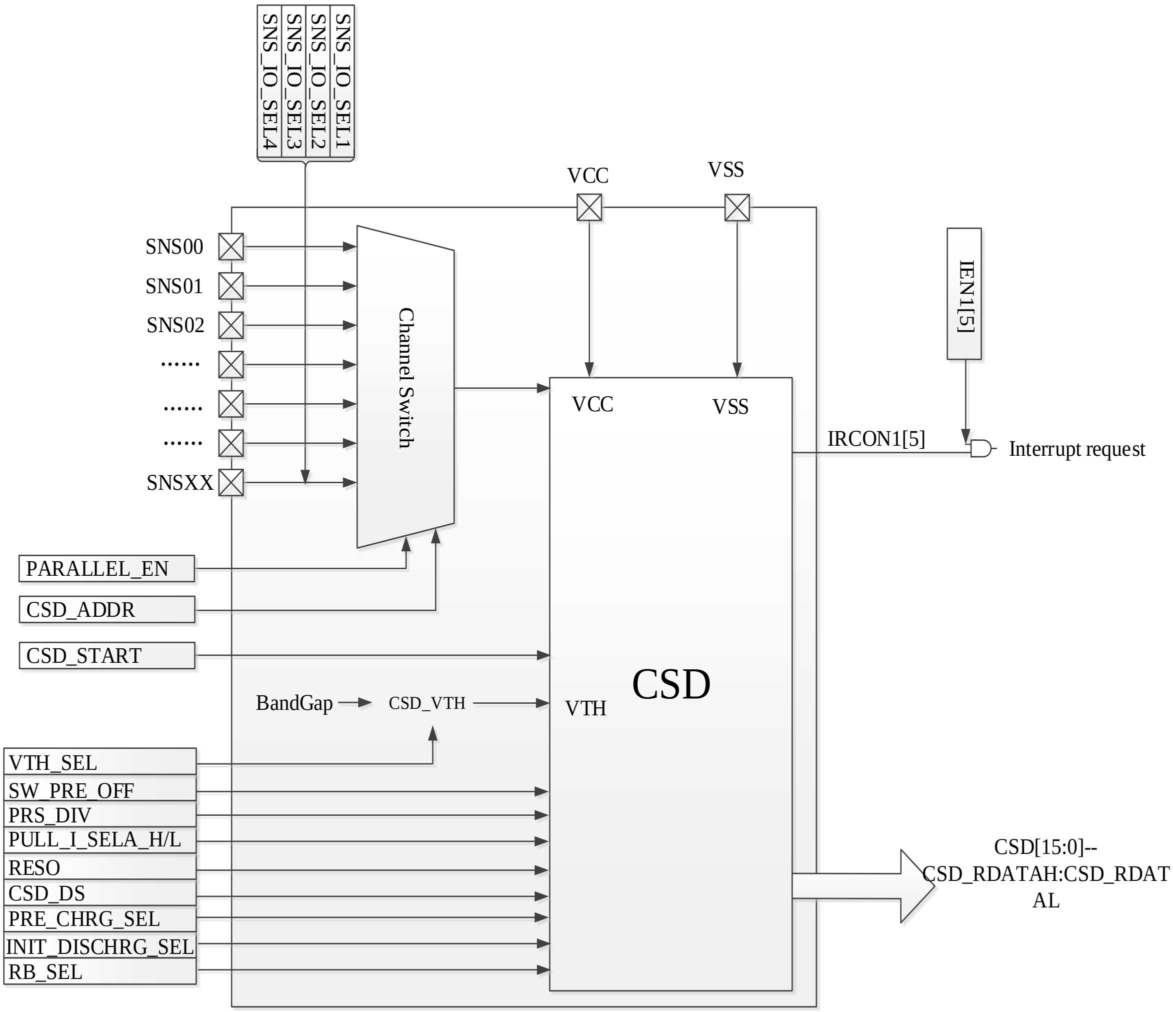
The signal-to-noise ratio of touch detection is proportional to VTH_SEL, and PULL_I_SELA_L, which is inversely proportional to CSD_DS. When the charge and discharge are incomplete, it is inversely proportional to the charge and discharge frequency set by PRS_DIV and the signal-to-noise ratio.

The detection time of a single button is related to RESO and CSD_DS.

Note: When configuring parameter, ensure that the keys are fully charged and discharged.

CSD schematic diagram of module structure:

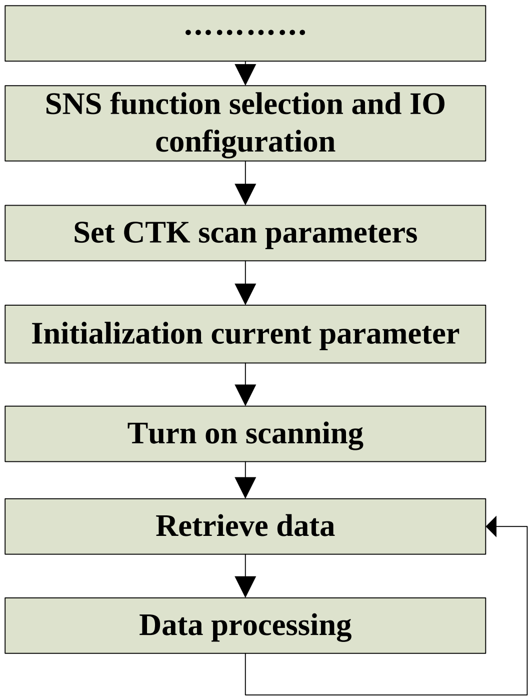




CSD structure diagram

12.3. CTK Configuration Process

The CTK button scan is a query or interrupt mode. First, configure the CTK parameters; then, turn on the CTK scan; finally, the CTK interrupts to obtain and save the CTK data, and the software algorithm performs data processing and button output judgment.



Touch button scan configuration flow chart

A set of parameters with a better signal-to-noise ratio can be obtained through the sensitivity parameter configuration, thereby improving the accuracy of button judgment.

1. **RESO:** 0~7 CTK capacitance scan resolution, counter digits: (RESO + 9) bits, the larger the CTK capacitance scan resolution is, the greater the amount of rawdata downward change is, and the noise introduced will increase accordingly, and vice versa.
2. **VTH_SEL:** 0~7**,** the smaller the reference voltage is, the greater the amount of change in Rawdata is, and the noise introduced will also increase, and vice versa.
3. **CSD_DS:** detection speed 0:24M, 1:12M, 2:6M, 3:4M, the smaller the detection speed is, the slower the rawdata sample time is, and vice versa. It is recommended that the default 24M is the fastest, and the detection speed is at least 2 times the PRS clock.
4. **RB_SEL:** RB resistance selection: 4: 60k; 5: 80k; The larger the resistance is, the greater the amount of change in Rawdata is, and the noise introduced will also increase, and vice versa.
5. **PRS_DIV**: Front-end charge and discharge clock frequency selection register:
   0~61: fixed frequency: F=F48M/2/(PRS_DIV/2+4) (6M~369K);
   62: The highest frequency 3M, the lowest frequency 1M, the center frequency 1.5M, normal distribution;
   63: The highest frequency 3M, the lowest frequency 1M, the center frequency 1.5M, uniform distribution;
   The larger the PRS clock is, the greater the variation of Rawdata is, and the noise introduced at the same time will increase, and vice versa.
6. **PULL_I_SELA_L:** Pull-up current source low 8 bits.
7. **PULL_I_SELA_H:** Pull-up current source high bit. Default value: 0x01.
   Current source size=255.5-0.5*{PULL_I_SELA_H, PULL_I_SELA_L}, the current source is smaller, the count value is smaller. Default value: 0x00.

Note:

1. Rawdata is the real-time raw count value of the CTK capacitance counter.
2. In actual applications, you need to view the data through the programming and debugging software and compare the parameters to get a set of parameters with good signal-to-noise ratio.
3. The relationship between chip supply voltage and reference voltage: VCC-VTH>0.5V.

12.4. CTK Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xCA	CSD_START	RW	xxxx_xxx0b	CSD scan open register
0xCB	SNS_SCAN_CFG1	RW	x000_0000b	Touch key scan configuration register 1
0xCC	SNS_SCAN_CFG2	RW	x100_0000b	Touch key scan configuration register 2
0xCD	SNS_SCAN_CFG3	RW	x111_0000b	Touch key scan configuration register 3
0xCE	CSD_RAWDATAL	R	0000_0000b	CSD count value low 8 bits
0xCF	CSD_RAWDATAH	R	0000_0000b	CSD count value high 8 bits
0xD1	PULL_I_SELA_L	RW	0000_0000b	CSD pull-up current source selection register
0xD2	SNS_ANA_CFG	RW	xx10_1111b	CSD scan parameter configuration register
0xD3	SNS_IO_SEL1	RW	0000_0000b	SNS channel selection register 1
0xD4	SNS_IO_SEL2	RW	0000_0000b	SNS channel selection register 2
0xD5	SNS_IO_SEL3	RW	0000_0000b	SNS channel selection register 3
0xD6	SNS_IO_SEL4	RW	xxxx_xx00b	SNS channel selection register 4
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xxx1_0111b	Module switch control register

CSD SFR register list

12.4.1. CSD Scan Open Register

CSD_START (CAH) CSD scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	1: CSD scan is started; 0: CSD scan is stopped Write 1 to CSD_START to start the scan, after one scan is over, the hardware will automatically set it to 0. To start the

		next scan, the software needs to set it to 1 again; if CSD_START=0 during the scan, then the scan will stop immediately, and the relevant signals inside the module will be reset. Note: It must be used according to the process configuration: CSD_START=1, when an interrupt is detected, configure CSD_START=0. Configuration of CSD_START is not allowed during scan

12.4.2. Touch Key Scan Configuration Register 1

SNS_SCAN_CFG1 (CBH) Touch key scan configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	SW_PRE_OFF	PRS_DIV					
R/W	-	R/W	R/W					
Reset value	-	0	0					

Bit number	Bit symbol	Description
6	SW_PRE_OFF	Front-end charge and discharge clock switch control. 1: Turn off sw_clk; 0: Turn on sw_clk
5~0	PRS_DIV	Front-end charge and discharge clock frequency selection register. 000000~ 111101: fixed frequency: F=F48M/2/(PRS_DIV+4)(6M~369K) 111110: The highest frequency is 3M, the lowest frequency is 1M, and the center frequency is 1.5M, normal distribution; 111111: The highest frequency is 3M, the lowest frequency is 1M, and the center frequency is 1.5M, uniform distribution

12.4.3. Touch Key Scan Configuration Register 2

SNS_SCAN_CFG2 (CCH) Touch key scan configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	PULL_I_SELA_H	PARALLEL_EN	CSD_ADDR				
R/W	-	R/W	R/W	R/W				
Reset value	-	1	0	0				

Bit number	Bit symbol	Description
6	PULL_I_SELA_H	CSD pull-up current source configuration highest bit
5	PARALLEL_EN	SNS channel parallel enable register

		1: Multi -channel parallel; 0: Single channel
4~0	CSD_ADDR	Address of the detection channel, corresponding to the channel number 0~25 00000: SNS0; 00001: SNS1; 00010: SNS2; 00011: SNS3; 00100: SNS4; 00101: SNS5; 00110: SNS6; 00111: SNS7; 01000: SNS8; 01001: SNS9; 01010: SNS10; 01011: SNS11; 01100: SNS12; 01101: SNS13; 01110: SNS14; 01111: SNS15; 10000: SNS16; 10001: SNS17; 10010: SNS18; 10011: SNS19; 10100: SNS20; 10101: SNS21; 10110: SNS22; 10111: SNS23; 11000: SNS24; 11001: SNS25; Others: Reserved

12.4.4. Touch Key Scan Configuration Register 3

SNS_SCAN_CFG3 (CDH) Touch key scan configuration register 3

Bit number	7	6	5	4
Symbol	-	RESO		
R/W	-	R/W		
Reset value	-	1	1	1
Bit number	3	2	1	0
Symbol	CSD_DS		PRE_CHRG_SEL	INIT_DISCHRG_SEL
R/W	R/W		R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~4	RESO	Counter bit selection register 000: 9 bits; 001: 10 bits; 010: 11 bits; 011: 12 bits; 100: 13 bits; 101: 14 bits; 110: 15 bits; 111: 16 bits.
3~2	CSD_DS	Count clock frequency selection register 00: 24M; 01: 12M; 10: 6M; 11: 4M; default: 0
1	PRE_CHRG_SEL	Precharge time selection: 0: 20 µs; 1: 40µs
0	INIT_DISCHRG_SEL	Pre-discharge time selection: 0: 2µs; 1: 10µs

12.4.5. CSD Count Value Registers

CSD_RAWDATAL (CEH) CSD count value low 8 bits

Bit number	7	6	5	4	3	2	1	0

Symbol	CSD_RAWDATAL[7:0]
R/W	R
Reset value	0

CSD_RAWDATAH (CFH) CSD count value high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	CSD_RAWDATAH[7:0]							
R/W	R							
Reset value	0							

12.4.6. CSD Pull-up Current Source Selection Register

PULL_I_SELA_L (D1H) CSD pull-up current source selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	PULL_I_SELA_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PULL_I_SELA_L[7:0]	CSD pull-up current source size selection switch; default is 0.

12.4.7. CSD Scan Parameter Configuration Register

SNS_ANA_CFG (D2H) CSD scan parameter configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	RB_SEL			VTH_SEL		
R/W	-	-	R/W			R/W		
Reset value	-	-	1	0	1	1	1	1

Bit number	Bit symbol	Description
5~3	RB_SEL	RB resistor size selection 100: 60k; 101: 80k; Others: Reserved When used, Rb80k calibration value needs to be read from chip Information: CBYTE[0x404D]k/ 80K to calculate the normalized sensitivity proportioned
2~0	VTH_SEL	VTH voltage selection signal, 000: 1.5V; 001: 2.1V; 010: 2.5V,

		011: 2.9V; 100: 3.2V; 101: 3.5V, 110: 3.9V; 111: 4.2V

12.4.8. SNS Channel Selection Registers

SNS_IO_SEL1 (D3H) SNS channel selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL1[7:0]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 00000001 = SNS0; 00000010 = SNS1; 00000100 = SNS2; 00001000 = SNS3; 00010000 = SNS4; 00100000 = SNS5; 01000000 = SNS6; 10000000 = SNS7

SNS_IO_SEL2 (D4H) SNS channel selection register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL2 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL2[7:0]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 00000001 = SNS8; 00000010 = SNS9; 00000100 = SNS10; 00001000 = SNS11; \ 00010000 = SNS12; 00100000 = SNS13; 01000000 = SNS14; 10000000 = SNS15

SNS_IO_SEL3 (D5H) SNS channel selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL3 [23:16]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description

7~0	SNS_IO_SEL3[23:16]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 00000001 = SNS16; 00000010 = SNS17; 00000100 = SNS18; 00001000 = SNS19; 00010000 = SNS20; 00100000 = SNS21; 01000000 = SNS22; 10000000 = NS23

SNS_IO_SEL4 (D6H) SNS channel selection register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	SNS_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	SNS_IO_SEL4[1:0]	SENSOR port selection enable bit 1: Select SENSOR; 0: Not select SENSOR 01 = SNS24; 10 = SNS25

12.4.9. Interrupt Related Registers

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	EX5	CSD interrupt enable 1: Interrupt enable; 0: Interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	IE5	CSD interrupt flag 1: With CSD interrupt flag; 0: No CSD interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	IPL1.5	CSD interrupt priority 0: Low priority 1: High priority;

12.4.10. Module Switch Control Register

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
1	PD_CSD	Simulate CSD work control register: 0: CSD module works normally; 1: CSD module does not work

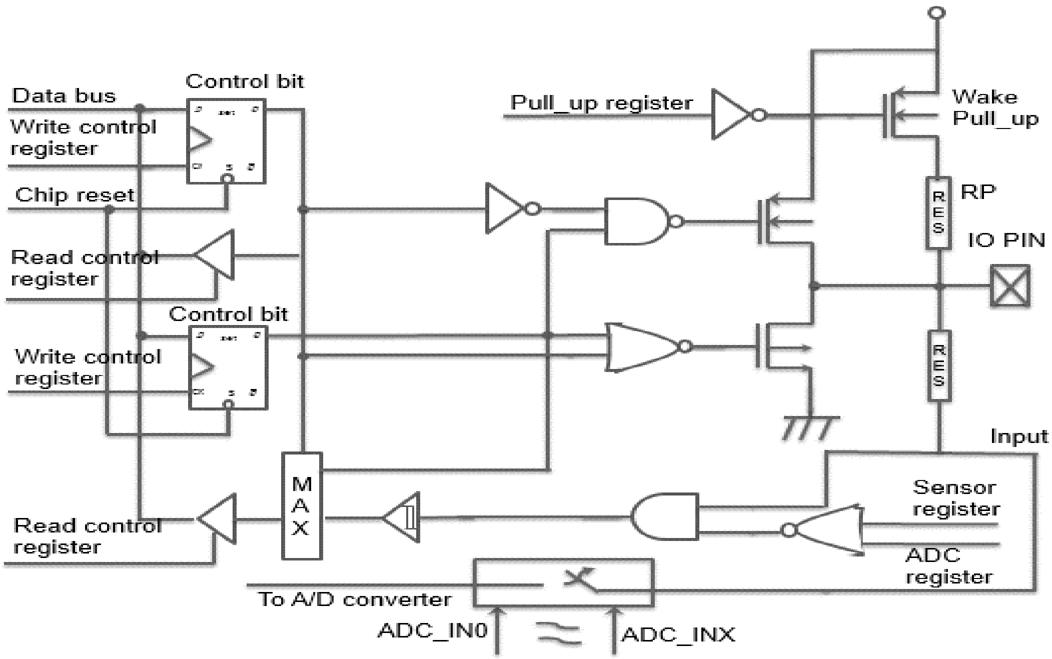
13. ADC

13. 1. Function Describe

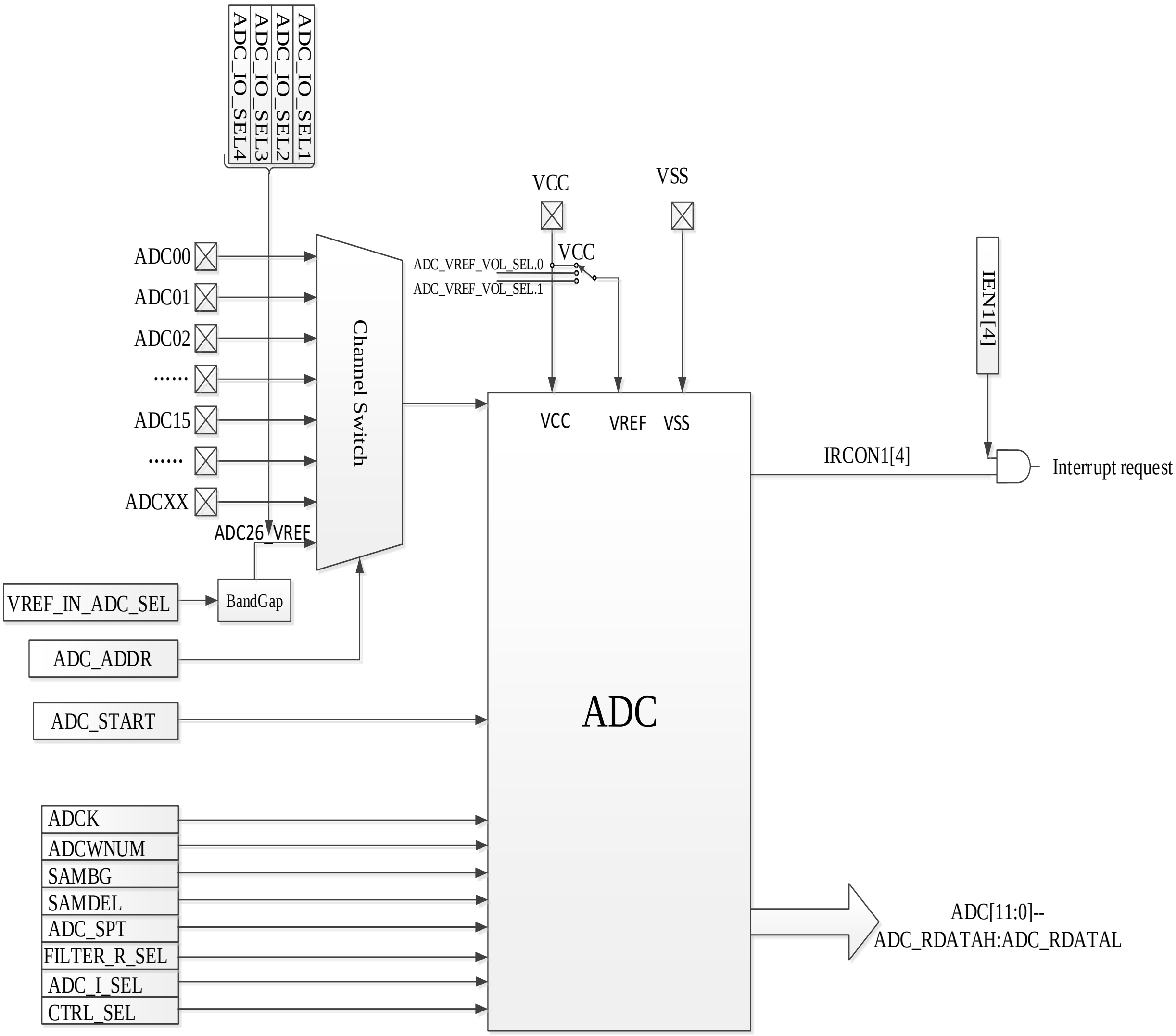
The BF7612DMXX-SJLX contains a single-ended, 12-bit linear successive approximation analog-to-digital converter (ADC), and the reference voltage of the ADC is connected to the VCC of the chip. ADC channels can input independent analog signals. The ADC module converts 1 channel each time, ADC_START=0→1( ) starts the conversion, after the conversion is completed, the ADC result register is updated and an interrupt is generated.

The ADC module of the BF7612DMXX-SJLX chip has the following features:

- 12-bit resolution linear and successive approximation to ADC
- Single conversion mode
- Sample time and conversion speed can be configured



ADC module structure diagram



ADC structure block diagram

13.1.1. ADC Detection Time

Timing requirement: (ADCWNUM+3) * Tadc_clk > 4 * Tadc_clk
Voltage settling time after ADC external input signal plus RC filtering >= 2*(ADC sample and conversion time)

The ADC detection time is divided into four parts:

1. Tsample: ADC sample time
2. T_2: Conversion interval time and sample delay time after ADC sampling
3. T_3: Time for ADC sampled signal to convert to data
4. T_4: ADC fixed time 200ns

The ADC detection time formula is as follows:

Parameter	Official
ADC conversion time	T_{AD} =Tsample+T_2+T_3+ T_4
Tsample	Tsample(μs) = 4*(ADC_SPT+1) *Tadc_clk
T_2	T_2=(ADCWNUM+3+SAMDEL)*T_{adc_clk}
T_3	T_3=(2*1+12)*T_{adc_clk}
T_4	T_4=200ns

ADC_CLK: ADC frequency division clock (3MHz/2MHz/1.5MHz/1MHz);
ADC_SPT: ADC sample time configuration register;
ADCWNUM: Selection of distance conversion interval time after sampling register;
SAMDEL: Sample delay time selection register.

13.1.2. ADC Reference Voltage

1. **When selecting VCC as the ADC reference voltage, when the power supply voltage fluctuates greatly or drops,**
   The VCC voltage value can be inversely calculated by the formula ADCINNER_Data/ VREF_IN_ADC_SEL = 4096/VCC,
   The Vin voltage value can be inversely calculated by the formula Vin_Data/Vin=4096/VCC.
   ADCINNER_Data: ADC26_VREF internal channel data;
   Vin_Data: ADC input channel data;
   Vin: Input voltage;
   VREF_IN_ADC_SEL: Need to read the chip calibration value,
   Vin = (Vin_Data/ADCINNER_Data)*VREF_IN_ADC_SEL, VREF_IN_ADC_SEL needs to read the chip calibration value, first obtain the internal channel data, and then obtain the input voltage Vin_Data data, and the interval between two data acquisitions should be as short as possible;
2. **When ADC_VREF_VOL _SEL 2V/4V reference voltage is selected,**
   It is recommended to select 3MHz for ADC frequency division clock,
   The voltage value of Vin can be inversely calculated by the formula

Vin_Data/Vin=4096/ADC_VREF_VOL _SEL.
Vin_Data: ADC input channel data;
Vin: Input voltage (0~ADC_VREF_VOL _SEL);
VREF_IN_ADC_SEL: Need to read the chip calibration value,
Vin = (Vin_Data/ADCINNER_Data)*VREF_IN_ADC_SEL, ADC_VREF_VOL _SEL needs to read the chip calibration value, Get the internal channel data first, then get the input voltage Vin_Data data, The interval between two data acquisitions should be as short as possible;

3. ADC calibration value:

CBYTE[0x4040] = ADC internal channel input voltage calibration value high 8 bits,
CBYTE[0x4041] = ADC internal channel input voltage calibration value low 8 bits,
Read the 1.433V calibration value of the chip's information address ADC internal channel input voltage;

CBYTE[0x4042] = ADC internal channel input voltage calibration value high 8 bits,
CBYTE[0x4043] = ADC internal channel input voltage calibration value low 8 bits,
Read the 2.388V calibration value of the chip's information address ADC internal channel input voltage;

CBYTE[0x4044] = ADC internal channel input voltage calibration value high 8 bits,
CBYTE[0x4045] = ADC internal channel input voltage calibration value low 8 bits,
Read the 3.306V calibration value of the chip's information address ADC internal channel input voltage;

CBYTE[0x4046] = ADC internal channel input voltage calibration value high 8 bits,
CBYTE[0x4047] = ADC internal channel input voltage calibration value low 8 bits,
Read the 4.297V calibration value of the chip's information address ADC internal channel input voltage;

CBYTE[0x4048] = ADC_VREF 2V voltage calibration value high 8 bits,
CBYTE[0x4049] = ADC_VREF 2V voltage calibration value low 8 bits,
Read the ADC_VREF 2V calibration value of the chip's information address;

CBYTE[0x404A] = ADC_VREF 4V voltage calibration value high 8 bits,
CBYTE[0x404B] = ADC_VREF 4V voltage calibration value low 8 bits,
Read the ADC_VREF 4V calibration value of the chip's information address;

13.1.3. ADC Interrupt

ADC input interrupt conditions:

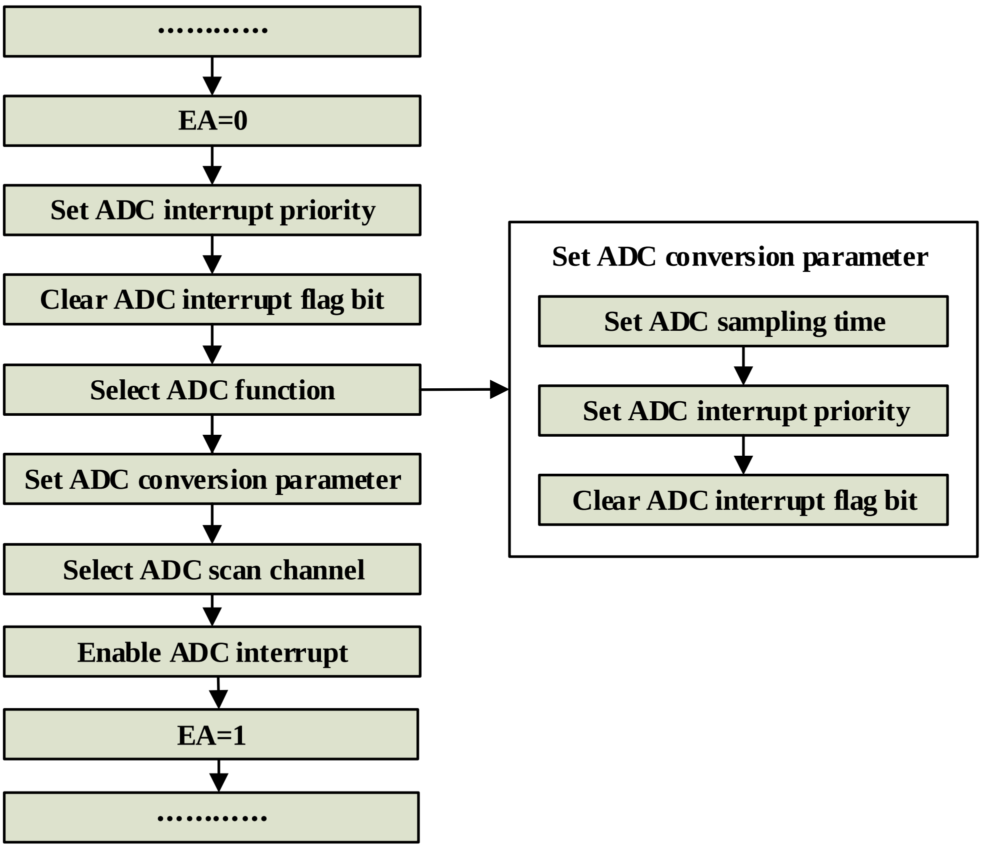
1. The configuration sequence is ADC_IO_SEL enable;
2. ADC interrupt enable;
3. ADC_ADDR (Address and ADC_IO_SEL must correspond);

4. ADC_START.

Note on initial configuration timing during application: If there is an application where ADC and IO port functions are multiplexed, you need to pay attention to the switching timing, If ADC_IO_SEL is enabled or disabled or address does not correspond to ADC_IO_SEL, ADC scanning cannot be turned on, and the configuration sequence must be followed: ADC_IO_SEL enable ->ADC interrupt enable->ADC_ADDR(Address and ADC_IO_SEL must correspond) -> ADC_START, t o enable ADC scan

When the pin is configured as ADC Function, the pin needs to be configured as IO input mode, and other multiplexing functions, are turned off, such as pull resistors.

13.2. ADC Configuration Process



ADC configuration flowchart

13.3. ADC Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xB4	ADC_SPT	RW	00000_0000b	ADC sample time configuration register
0xB5	ADC_SCAN_CFG	RW	xx00_0000b	ADC scan control register
0xB6	ADCCKC	RW	xxxx_xx00b	ADC Clock control register
0xB9	ADC_RDATAH	R	xxxx_0000b	ADC scan result register high 4 bits
0xBA	ADC_RDATAL	R	0000_0000b	ADC scan result register low 8 bits
0xBB	ADC_CFG1	RW	0000_0000b	ADC sample sequence control register 1
0xBC	ADC_CFG2	RW	x000_111xb	ADC sample sequence control register 2
0xD9	ADC_IO_SEL1	RW	0000_0000b	ADC select enable register 1
0xDA	ADC_IO_SEL2	RW	0000_0000b	ADC select enable register 2
0xDB	ADC_IO_SEL3	RW	0000_0000b	ADC select enable register 3
0xDC	ADC_IO_SEL4	RW	xxxx_xx00b	ADC select enable register 4
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xxx1_0111b	Module switch control register

ADC SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x2D	ADC_CFG_SEL	RW	xxxx_xx00b	ADC control register

13.3.1. ADC Sample Time Configuration Register

ADC_SPT (B4H) ADC sample time configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT	ADC sample time configuration register Sample time: Tsample = (ADC_SPT+1)*4*Tadc_clk

13.3.2. ADC Scan Control Register

ADC_SCAN_CFG (B5H) ADC scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	ADC_ADDR					ADC_START
R/W	-	-	R/W					R/W
Reset value	-	-	0					0

Bit number	Bit symbol	Description
5~1	ADC_ADDR	ADC channel address selection register 00000: Corresponding to ADC0; 00001: Corresponding to ADC1; …… 11000: Corresponding to ADC24; 11001: Corresponding to ADC25; 11010: Corresponding to ADC26_VREF； Reserved all other values
0	ADC_START	ADC scan open register: 0: ADC module does not scan; 1: ADC module starts to scan ADC_START is set from 0 to 1. ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit. The ADC interrupt flag bit needs to be cleared by software. Note: ADC_START is not allowed to be configured during scanning

13.3.3. ADC Clock Control Register

ADCCKC (B6H) ADC clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADCK	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
7~2	--	Reserved
1~0	ADCK	ADC_CLK frequency division selection 0: 3MHz 1: 2MHz 2: 1.5MHz 3: 1MHz

13.3.4. ADC Scan Result Registers

ADC_RDATAH (B9H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RDATAH[3:0]			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	ADC_RDATAH[3:0]	ADC scan result register

ADC_RDATAL (BAH) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_RDATAL[7:0]	ADC scan result register

13.3.5. ADC Sample Sequence Control Register 1

ADC_CFG1 (BBH) ADC sample sequence control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADCWNUM					SAMBG	SAMDEL	
R/W	R/W					R/W	R/W	
Reset value	0					0	0	

Bit number	Bit symbol	Description
7~3	ADCWNUM	Selection of distance conversion interval time after sampling 00000: Reserved; 00001: Reserved; 00010: 5 ADC_CLK; 00011: 6 ADC_CLK; 00100: 7 ADC_CLK; …… 11110: 33 ADC_CLK; 11111: 34 ADC_CLK;
2	SAMBG	Sample timing and comparison timing interval selection 0: Interval of 0 ADC_CLK; 1: Interval of 1 ADC_CLK
1~0	SAMDEL	Sample delay time selection 00: 0 ADC_CLK; 01: 2 ADC_CLK; 10: 4 ADC_CLK;

		11: 8 ADC_CLK

13.3.6. ADC Sample Sequence Control register 2

ADC_CFG2 (BCH) ADC sample sequence control register 2

Bit number	7	6	5	4
Symbol	-	FILTER_R_SEL	VREF_IN_ADC_SEL	
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	ADC_I_SEL[1:0]		CTRL_SEL	-
R/W	R/W	R/W	R/W	-
Reset value	1	1	1	-

Bit number	Bit symbol	Description
6	FILTER_R_SEL	Input signal filter selection 0: No filtering; 1: Add 10K resistance filter, default value is 0
5~4	VREF_IN_ADC_SEL	Voltage selection for reference voltage input to ADC26_VREF 00: 1.433V; 01: 2.388V; 10: 3.306V; 11: 4.297V
3	ADC_I_SEL[1]	Operational amplifier bias current size selection signal 0 is 1 uA; 1 is 2uA. The default value is 1
2	ADC_I_SEL[0]	Comparator bias current size selection signal 0 is 1 uA; 1 is 2uA. The default value is 1
1	CTRL_SEL	Comparator maladjustment eliminates selection signals 0: Sample and then dissonance elimination; 1: All switches are turned off. The default value is 1
0	--	Reserved

13.3.7. ADC Select Enable Registers

ADC_IO_SEL1 (D9H) ADC select enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1[7:0]							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1[7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001 = ADC00; 00000010 = ADC01; 00000100 = ADC02; 00001000 = ADC03; 00010000 = ADC04; 00100000 = ADC05; 01000000 = ADC06; 10000000 = ADC07

ADC_IO_SEL2 (DAH) ADC select enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2[7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001 = ADC08; 00000010 = ADC09; 00000100 = ADC10; 00001000 = ADC11; 00010000 = ADC12; 00100000 = ADC13; 01000000 = ADC14; 10000000 = ADC15

ADC_IO_SEL3 (DBH) ADC select enable register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3[7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001 = ADC16; 00000010 = ADC17; 00000100 = ADC18; 00001000 = ADC19; 00010000 = ADC20; 00100000 = ADC21;

		01000000 = ADC22; 10000000 = ADC23

ADC_IO_SEL4 (DCH) ADC select enable register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	ADC_IO_SEL4[1:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 01 = ADC24; 10 = ADC25

13.3.8. Interrupt Related Registers

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	EX4	ADC interrupt enable 1: Interrupt enable; 0: Interrupt disable;

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	IE4	ADC interrupt flag 1: With interrupt flag; 0: No interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-

R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	IPL1.4	ADC interrupt priority 0: Low priority; 1: High priority

13.3.9. Module Switch Control Register

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
0	PD_ADC	Analog ADC shut down control register: 0: ADC module works normally; 1: ADC module does not work

13.3.10. Secondary Bus Registers

ADC_CFG_SEL (2DH) ADC control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_VREF_SEL	ADC_VREF_VOL_SEL
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	ADC_VREF_VOL_SEL	ADC_VREF output mode selection signal. 0: 2V is used as ADC reference voltage 1: 4V is used as ADC reference voltage
0	ADC_VREF_SEL	Select the source of the output signal. 0: Select VCC as the output signal 1: Select the output of ADC_VREF module as the output signal

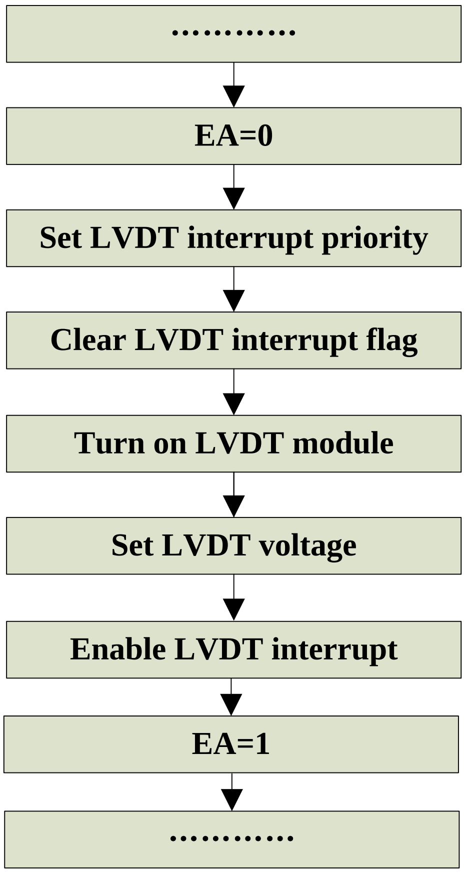
14. LVDT

14.1. Function Describe

The BF7612DMXX-SJLX series supports low voltage alarm function, which can effectively monitor the dynamic changes of voltage. Support 6 voltage levels, respectively: 2.7V/3.0V/3.3V/3.6V/3.9V/4.2V (preset point step-down interrupt, hysteresis 0.1V generates corresponding step-up interrupt).

When the voltage monitoring is configured with the above threshold, the voltage drop to this threshold will trigger a low-voltage interrupt, and the system can handle the low-voltage interrupt appropriately according to application needs.

14.2. LVDT Configuration Process



LVDT configuration flow chart

14.3. LVDT Related Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT power-on/brown-out interrupt status register
0xE1	IRCON2	RW	xxxx_0000b	Interrupt flag register 2
0xE7	IEN2	RW	xxxx_0000b	Interrupt enable register 2
0xF4	IPL2	RW	xxxx_0000b	Interrupt priority register 2
0xFE	PD_ANA	RW	xxx1_0111b	Module switch control register
0xFF	BOR_LVDT_VTH	RW	xx00_0000b	BOR and LVDT threshold select register

LVDT SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x2E	BOR_LVDT_DEALY_SEL	RW	xxxx_x000	BOR and LVDT delay selection register

14.3.1. Interrupt Related Registers

INT_POBO_STAT (86H) LVDT power-on/brown-out interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	LVDT power-on interrupt status 1: Power-on interrupt is valid; 0: Power-on interrupt is invalid.
0	INT_BO_STAT	LVDT brown-out interrupt status 1: Brown-out interrupt is valid; 0: Brown-out interrupt is invalid

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IE11	IE10	IE9	IE8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description

0	IE8	LVDT interrupt flag 1: With interrupt flag 0: No interrupt flag

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EX11	EX10	EX9	EX8
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
0	EX8	LVDT interrupt enable 1: Interrupt enable; 0: Interrupt disable;

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
0	IPL2.0	LVDT interrupt priority 0: Low priority; 1: High priority

14.3.2. Module Switch Control Register

PD_ANA (FEH) Module switch control register

Bit number	7~5	4	3	2	1	0
Symbol	-	PD_LVDT	PD_BOR	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	1	0	1	1	1

Bit number	Bit symbol	Description
4	PD_LVDT	LVDT control register 1: Close, 0: Open, closed by default

14.3.3. LVDT Threshold Select Register

BOR_LVDT_VTH ( ) BOR and LVDT threshold select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	SEL_BOR_VTH[2:0]			SEL_LVDT_VTH[2:0]		
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
2~0	SEL_LVDT_VTH[2:0]	LVDT threshold select 00: Reserved; 001: 2.7V; 010: 3.0V; 011: 3.3V; 100: 3.6V; 101: 3.9V; 11x: 4.2V

14.3.4. LVDT Delay Selection Register

BOR_LVDT_DEALY_SEL (2EH) BOR and LVDT delay selection register (Secondary bus register)

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	BOR_DELAY_SEL	LVDT_DELAY_SEL	
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
1~0	LVDT_DELAY_SEL	LVDT delay selection 00: Delay time 1; 01: Delay time 2; 10: Delay time 3; 11: Delay time 4

Threshold select <2:0>	Delay time Xselection <1:0>	Brown-out threshold (V)	Restore threshold (V)	Hysteresis voltage (mV)	Delay time (us)
001	00	2.7	2.8	120.9	7.7
	01	2.7	2.8	121.2	15.4
	10	2.7	2.8	121.9	31.1
	11	2.7	2.8	123.3	62.5
010	00	3.0	3.1	112.8	9.1
	01	3.0	3.1	113.2	18.4
	10	3.0	3.1	114.1	37.5
	11	3.0	3.1	115.8	75.5
011	00	3.3	3.4	134.1	10.3
	01	3.3	3.4	134.6	21
	10	3.3	3.4	135.6	42.9
	11	3.3	3.4	137.5	86.7
100	00	3.6	3.7	107.5	11.7
	01	3.6	3.7	108	24
	10	3.6	3.7	109.2	49.3
	11	3.6	3.7	111.4	99.7
101	00	3.9	4.0	124.2	12.9
	01	3.9	4.0	124.8	26.6
	10	3.9	4.0	126.1	54.6
	11	3.9	4.0	128.6	110.6
11X	00	4.2	4.3	120.7	14.3
	01	4.2	4.3	121.4	29.5
	10	4.2	4.3	122.8	60.7
	11	4.2	4.3	125.6	123.2

15. LED

The main functions of LED dot matrix drive mode:

- Supports up to 64 lights LED drive, configurable to choose matrix 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8 dual lights at the same time on mode, the specific allocation see the matrix description below
- Single lamp on-time setting file: 8-bit register, configurable range is 16μs-4.096ms, step is 16μs;
- Each lamp driving time is individually selectable;
- IO ports have multiple multiplexing relationships. Each IO port needs to be configured through software to switch to LED port. According to the LED dot matrix mode selection, the LED function of LED0~LED8 corresponding to IO port will be automatically turned on. The starting port LED0 supports the selection of PB0~PB7, PC0. Other mouth sequence circulation;
- 64 light dot matrix address is unique, see the dot matrix description below, used to input switch light information;
- Support wait mode interrupt to wake up the system
- Support high current drive of 8 GPIO ports

15.1. Function Description

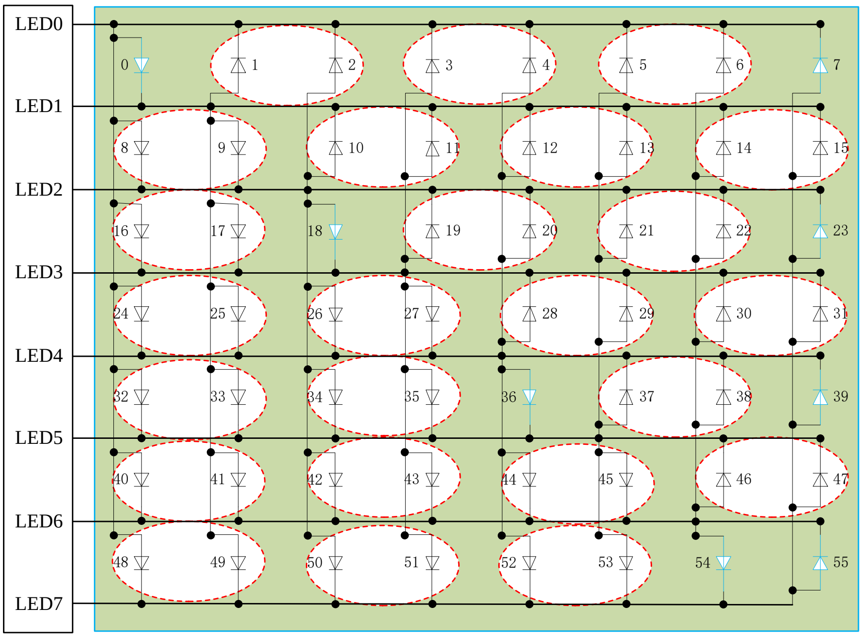
15.1.1. LED

The LED dot matrix drive circuit consists of a controller, two counters, a comparator and a SRAM storage circuit.

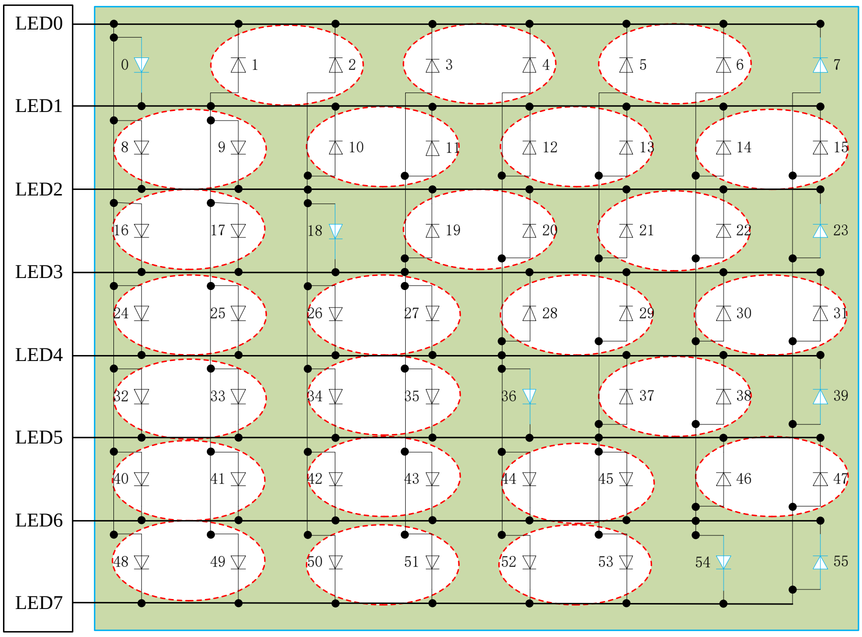
The LED dot matrix is a general 8*8 matrix dual-lamp scanning mode, that is, two lamps (common cathode) are lit at a time.

Corresponding to LED0~LED8 ports, up to 8x8 = 64 lamps can be configured to drive. The address of the corresponding position lamp is marked in the 8*8 matrix below, and the display configuration in sram corresponds to the lighting condition of the corresponding address (1 means lighting, 0 means no light), the hardware code needs to analyze the lighted address and the current scanning address to automatically complete the corresponding IO port output control.
Configurable matrix 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8, different size matrix, the corresponding lamp Address remains unchanged.

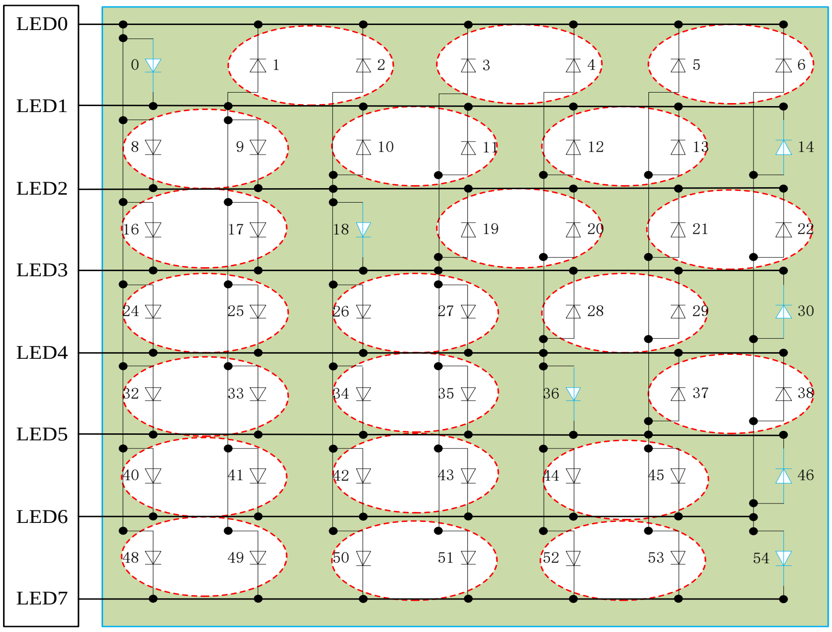
8*8 matrix:



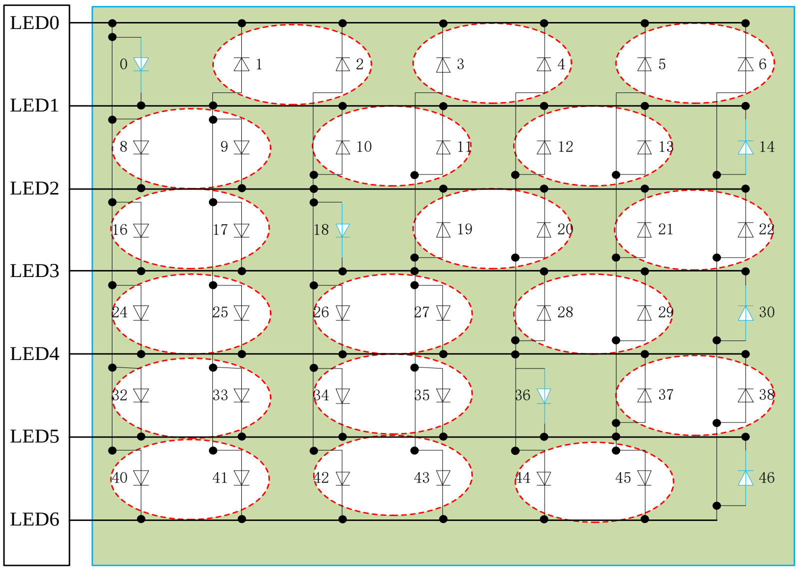
7*8 matrix:



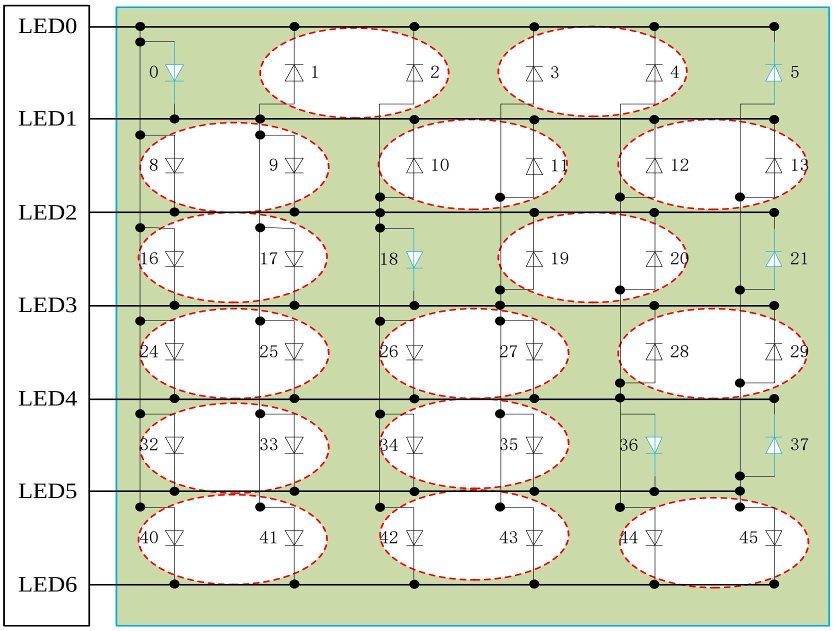
7*7 matrix:



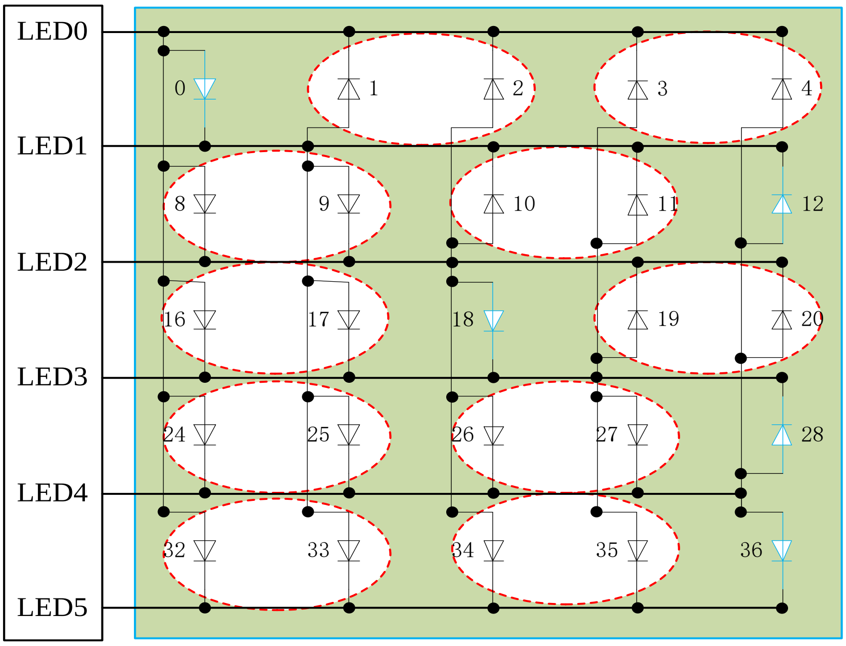
6*7 matrix:



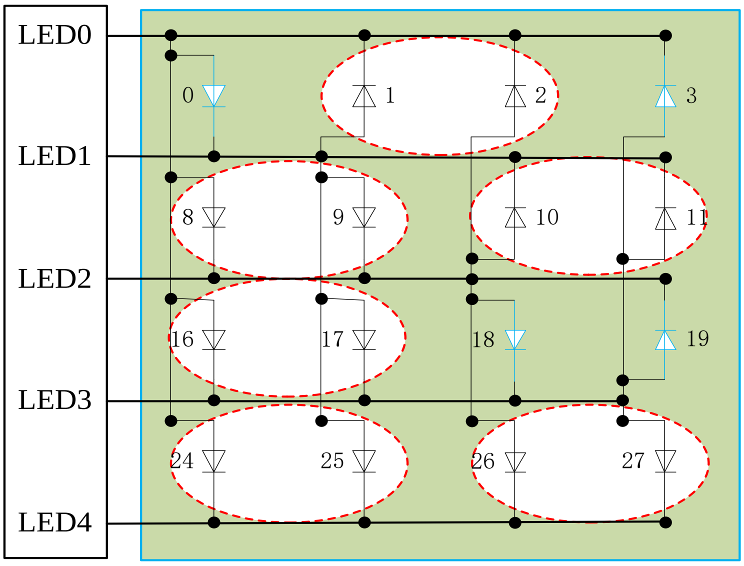
6*6 matrix:



5*5 matrix:

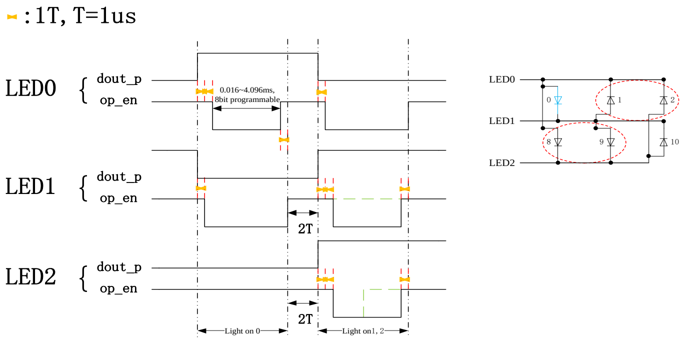


4*4 matrix:



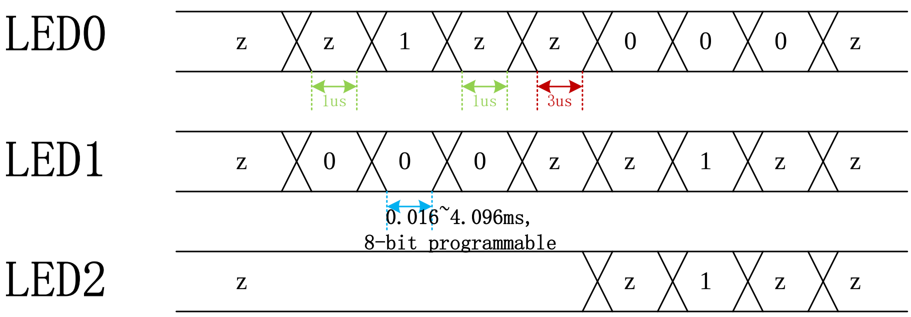
Dot matrix scan timing example:

Take lighting 0, 1, 2 as an example, the detailed digital output interface control sequence is shown in the figure below:



1. dout_p: Outputs data signals
2. op_en: Outputs the enabling signal

Combined with the above figure, the schematic diagram of the IO port status is as follows:



15.2. Drive Current

（Ta = 25℃, VCC = 5V, LED voltage drop 2.3V)

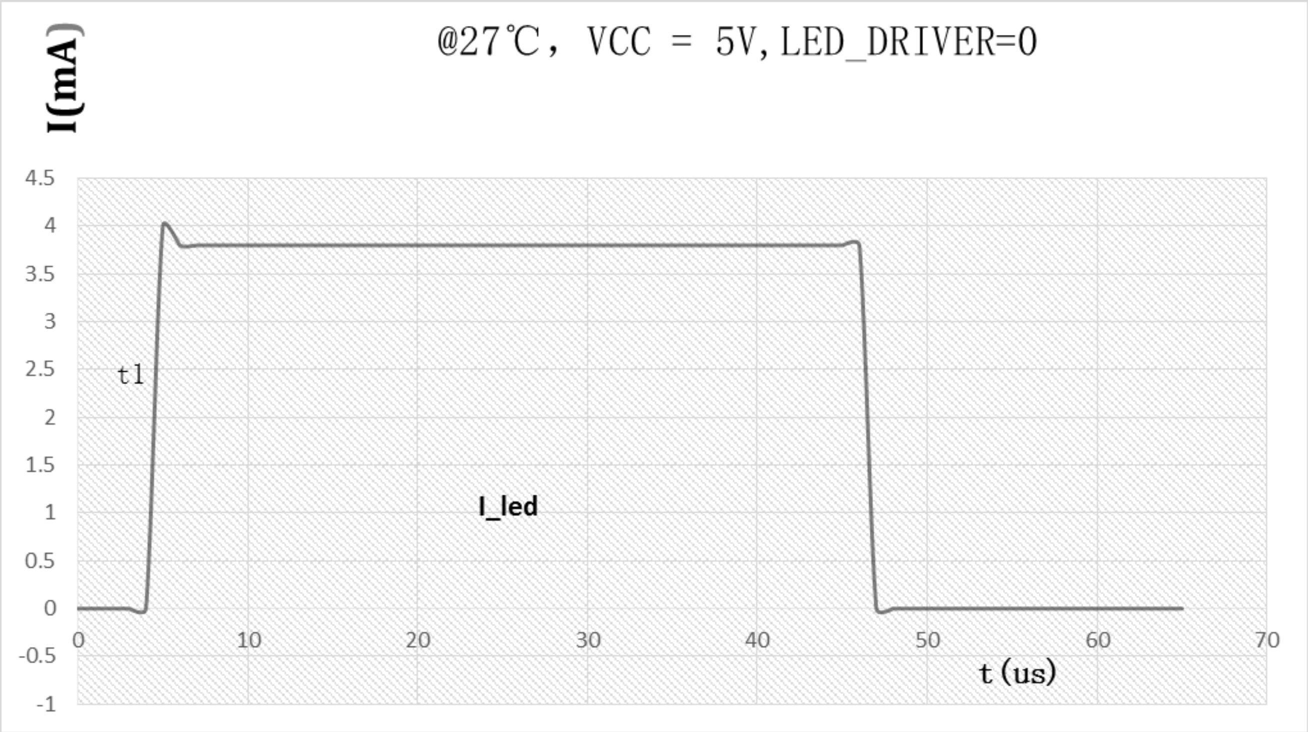
LED_DRIVE	I_led current (mA)
0	**3.8**
1	8.5
2	13.1
3	17.7
4	22.2
5	26.7
6	31.0
7	35.4
8	39.8
9	44.0
10	48.3
11	52.6
12	56.8
13	61.0
14	65.0
15	69.1

LED secondary bus drive current configuration register reference list

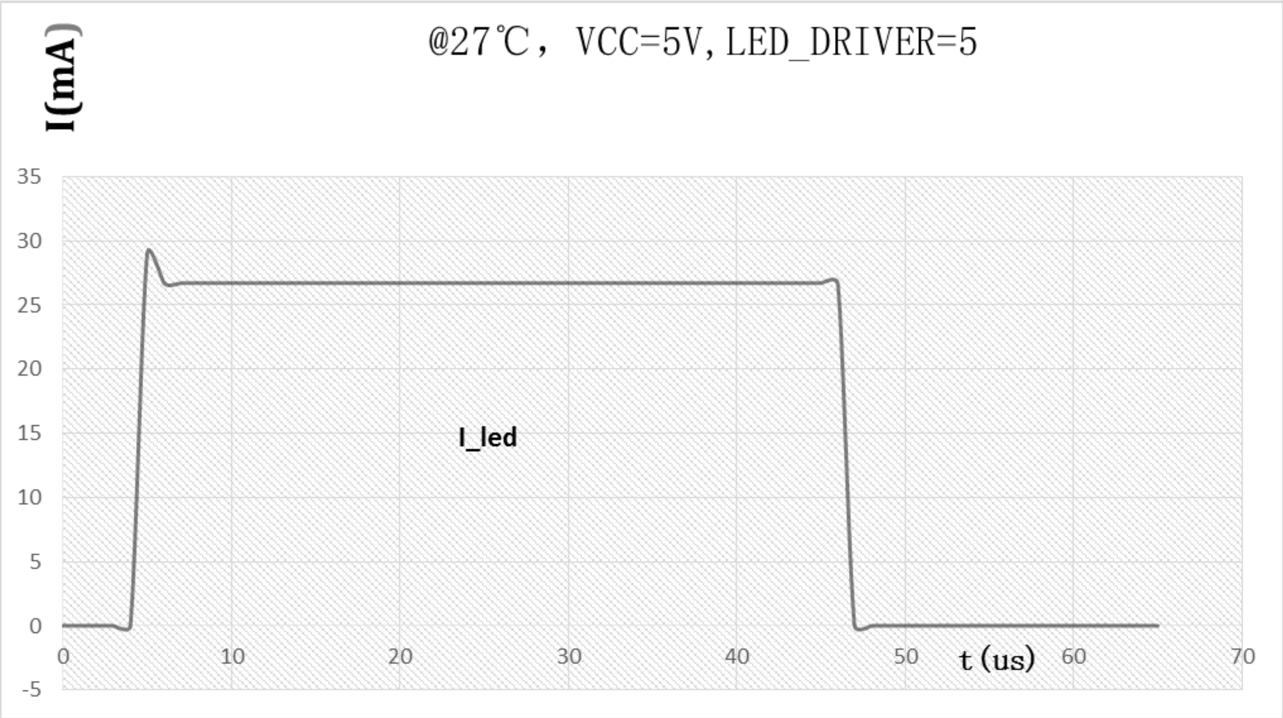
Note:

1. LED drive current deviation range (±8%)@VCC=5V, Ta=(-40°C~105°C), the setting of LED_DRIVE is recommended to be less than the nominal Ifp current of the LED lamp, and the LED lamp to be driven should be forward LED lights with the same voltage V_F.
2. LED_DRIVE: LED driver capability configuration register;
3. I_led: LED light conducts steady-state current.

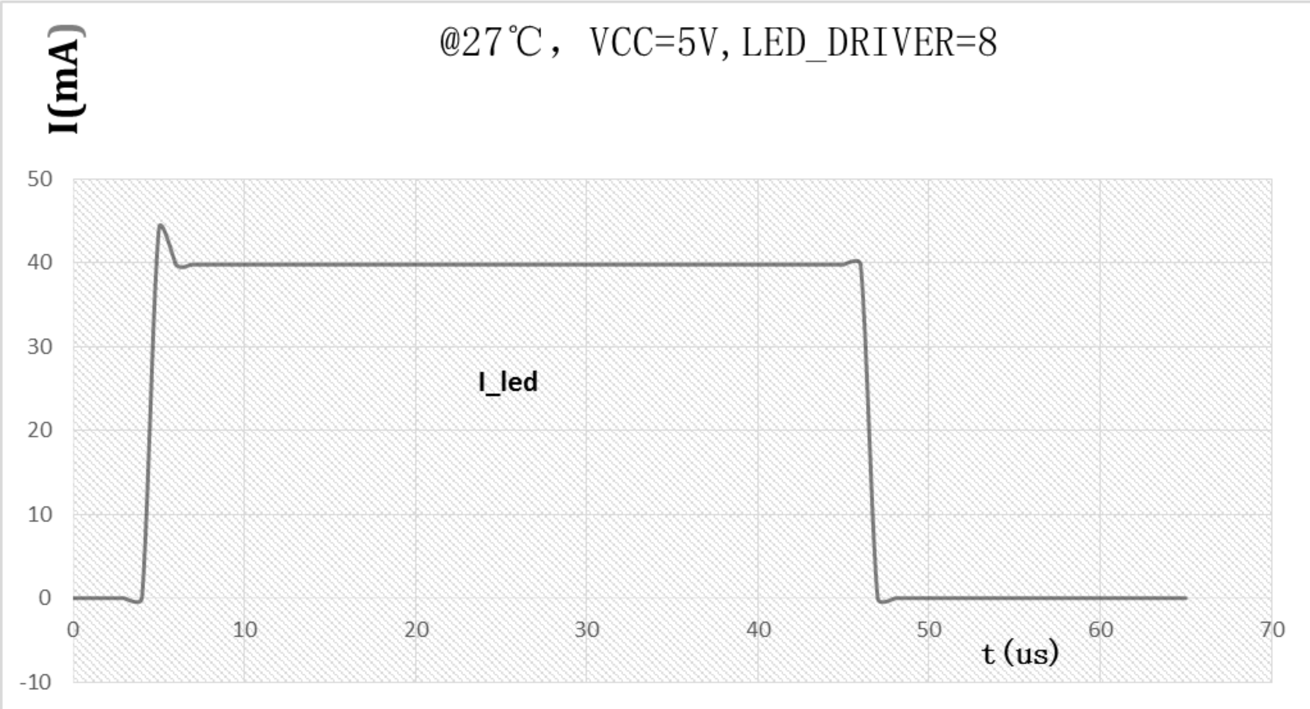
LED serial dot matrix drive current-time diagram under several common configurations:



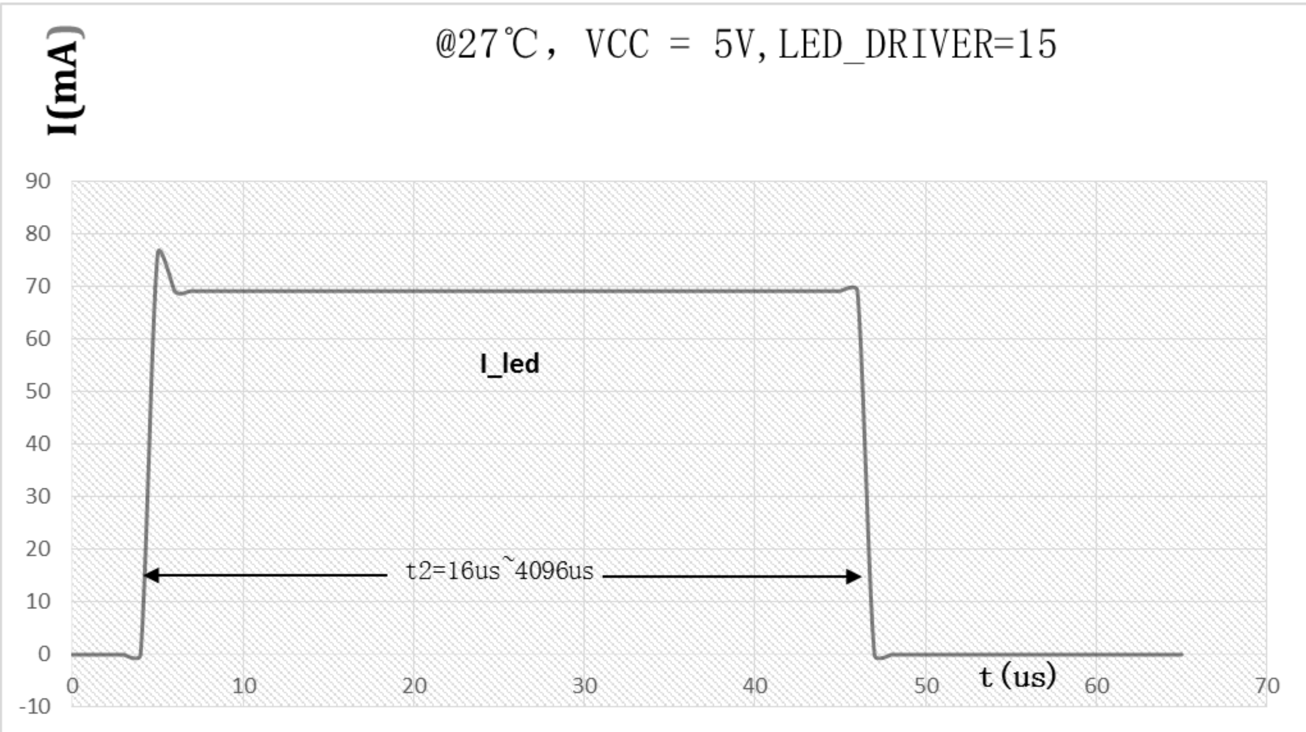
LED_DRIVER VS Time Figure1



LED_DRIVER VS Time Figure2



LED_DRIVER VS Time Figure3



LED_DRIVER VS Time Figure4

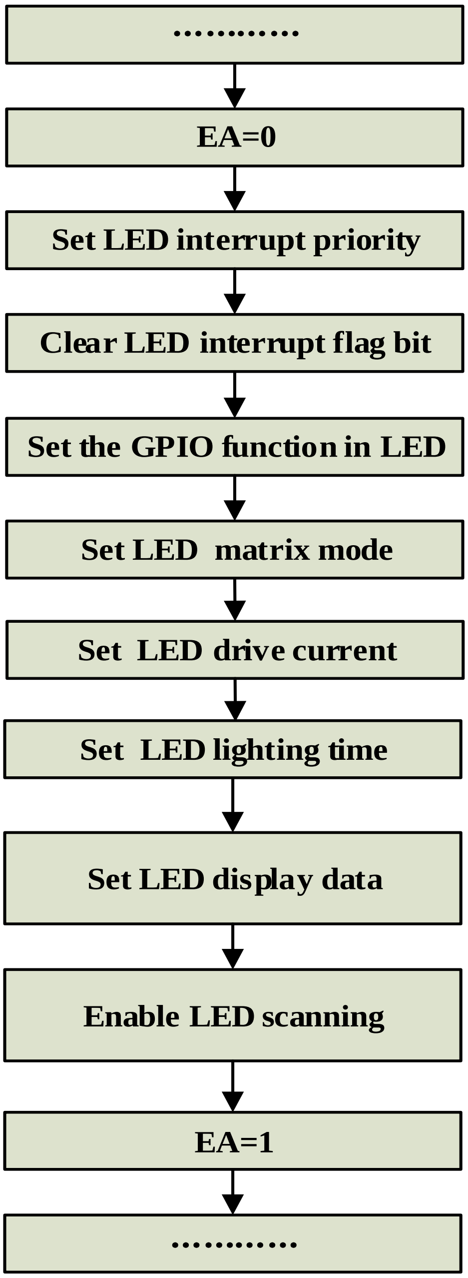
15.3. Display Configuration Address

LED dot matrix drive mode corresponding to display configuration:
DX indicates whether the light is selected or not, 0: not bright, 1: bright;
Dx_SEL indicates that the light is selected for the lighting cycle, 0: select the first segment of the light cycle, 1: select the second segment of the light cycle.

Address	7	6	5	4	3	2	1	0
200H	D7	D6	D5	D4	D3	D2	D1	D0
201H	D15	D14	D13	D12	D11	D10	D9	D8
202H	D23	D22	D21	D20	D19	D18	D17	D16
203H	D31	D30	D29	D28	D27	D26	D25	D24
204H	D39	D38	D37	D36	D35	D34	D33	D32
205H	D47	D46	D45	D44	D43	D42	D41	D40
206H	D55	D54	D53	D52	D51	D50	D49	D48
207H	D63	D62	D61	D60	D59	D58	D57	D56
208H	D7_SEL	D6_SEL	D5_SEL	D4_SEL	D3_SEL	D2_SEL	D1_SEL	D0_SEL
209H	D15_SEL	D14_SEL	D13_SEL	D12_SEL	D11_SEL	D10_SEL	D9_SEL	D8_SEL
20AH	D23_SEL	D22_SEL	D21_SEL	D20_SEL	D19_SEL	D18_SEL	D17_SEL	D16_SEL
20BH	D31_SEL	D30_SEL	D29_SEL	D28_SEL	D27_SEL	D26_SEL	D25_SEL	D24_SEL
20CH	D39_SEL	D38_SEL	D37_SEL	D36_SEL	D35_SEL	D34_SEL	D33_SEL	D32_SEL
20DH	D47_SEL	D46_SEL	D45_SEL	D44_SEL	D43_SEL	D42_SEL	D41_SEL	D40_SEL
20EH	D55_SEL	D54_SEL	D53_SEL	D52_SEL	D51_SEL	D50_SEL	D49_SEL	D48_SEL
20FH	D63_SEL	D62_SEL	D61_SEL	D60_SEL	D59_SEL	D58_SEL	D57_SEL	D56_SEL

LED dot matrix drive mode corresponding display configuration table

15.4. LED Configuration Process



LED configuration flow chart

15.5. LED Related Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xAF	SCAN_START	RW	xxxx_xxx0b	LED scan open register
0xB0	DP_CON	RW	xxx0_0000b	LED scan control register
0xB1	SCAN_WIDTH	RW	0000_0000b	LED scan on time 1 control register
0xB2	LED2_WIDTH	RW	0000_0000b	LED scan on time 2 control register
0xB3	LED_DRIVE	RW	xxxx_0000b	LED driver capability configuration register
0xC4	LED_IO_START	RW	xxxx_0000b	LED start port control register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xEE	COM_IO_SEL	RW	0000_0000b	COM port selection configuration register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

LED SFR register list

15.5.1. LED Scan Open Register

SCAN_START (AFH) LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LED scan open register 1: Scan open; 0: Scan close; In interrupt mode, the scan starts after the configuration is enabled. After that, the hardware is automatically cleared until the software configuration is enabled again. The software can also be directly configured and shut down In cyclic mode, the configuration remains unchanged after it is enabled until the software configuration is closed (the oftware ends immediately) and related signals inside the Module are reset

15.5.2. LED Scan Control Register

DP_CON (B0H) LED scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	DUTY_SEL			SCAN_MODE	COM_MOD
R/W	-	-	-	R/W			R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
4~2	DUTY_SEL	LED port drive mode matrix selection configuration register 0: No matrix 1: 4x4 matrix(LED0~LED4); 2: 5x5 matrix(LED0~LED5); 3: 6x6 matrix(LED0~LED6); 4: 6x7 matrix(LED0~LED6); 5: 7x7 matrix(LED0~LED7); 6: 7x8 matrix(LED0~LED7); 7: 8x8 matrix(LED0~LED8)
1	SCAN_MODE	LED scan mode configuration 1: Cycle scan mode 0: Interrupt scan mode
0	COM_MOD	High current sink IO port drive enable 1: The COM locking function, as large current IO mouth work 0: The COM port is not locked and can be configured for other functions When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED scan configuration is invalid

15.5.3. LED Scan on Time 1 Control Register

SCAN_WIDTH (B1H) LED scan on time 1 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In LED dot matrix drive mode, corresponding to a single indicator time configuration register——Conduction time 1 set period=(scan_width+1)*16us, supports the configuration range0.016~4.096ms

15.5.4. LED Scan on Time 2 Control Register

LED2_WIDTH (B2H) LED scan on time 2 control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In LED dot matrix drive mode, corresponding to a single indicator time configuration register——Conduction time 2 set period=(led2_width+1)*16us, supports the configuration range0.016~4.096ms

15.5.5. LED Driver Capability Configuration Register

LED_DRIVE (B3H) LED driver capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-			
R/W	-	-	-	-	R/W			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
7~0	--	LED port drive capability configuration register 0~15—3.77mA~69.14mA, refer to the LED drive ammeter for details.

15.5.6. LED Start Port Control Register

LED_IO_START (C4H) LED start port control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	LED_IO_START[3:0]			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	LED_IO_START[3:0]	LED port matrix start PAD selection 0000: PB0; 0001: PB1;

		0010: PB2; 0011: PB3; 0100: PB4; 0101: PB5; 0110: PB6; 0111: PB7; 1000: PC0; Others: PB0;

15.5.7. Interrupt Related Registers

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
6	EX6	LED interrupt enable 1: Interrupt enable; 0: Interrupt disable;

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
6	IE6	LED interrupt flag 1: With interrupt flag 0: No interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
6	IPL1.6	LED priority 0: Low priority; 1: High priority

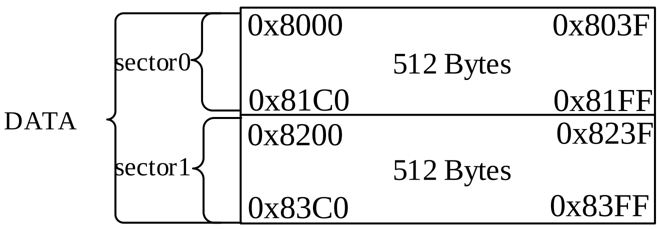
16. DATA Area

16.1. Function Overview

The DATA area is 1K Bytes and divided into 2 sectors, each of which is divided into 4 pages. The DATA area needs to be erased when it is used, and then the word burn operation is carried out. After erased, it can only be written once.

The DATA area supports block erase, sector erase, page erase, and word programming operations. The size of each erase is shown in the following table:

DATA area	Block erase	Sector erase	Page erase
Erase space size	1K Bytes	512 Bytes	128 Bytes



{SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} The logical address (0~1023) corresponds to the physical address (0x8000~0x83FF)

16.2. Block Erase Steps

1. SPROG_TIM[4:0] = 2~25 (suggest 5ms), configure SPROG_TIM[7:5] = 0 and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_L = 0x00;
4. Configure SPROG_ADDR_H = 0x00;
5. Configure SPROG_CMD = 0x94
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after erasing is completed;

16.3. Sector Erase Steps

1. SPROG_TIM[4:0] = 2~25 (suggest 5ms), configure SPROG_TIM[7:5] = 0 and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_L = 0x00;
4. Configure SPROG_ADDR_H = 0x00; (Sector0)
   (SPROG_ADDR_H [1]: 0 indicates Sector0, 1 indicates Sector1. and select the sector to be erased)
5. Configure SPROG_CMD = 0x96;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after erasing is completed;
8. Need to continue writing data, jump to step 3;
9. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings;

16.4. Page Erase Steps

1. SPROG_TIM[4:0] = 2~25 (suggest 5ms), configure SPROG_TIM[7:5] = 0 and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_L = 0x00;
4. Configure SPROG_ADDR_H = 0x00 (page0)
   ({SPROG_ADDR_H[1:0] , SPROG_ADDR_L[7]} is used to select pages 0 to 7 and select pages to be erased);
5. Configure SPROG_CMD = 0x95;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after erasing is completed;
8. Need to continue writing data, jump to step 3;
9. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings;

16.5. Word Burn Write Steps

1. SPROG_TIM[4:0] = 2~25 (suggest 5ms), configure SPROG_TIM[7:5] = 0 and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_H, SPROG_ADDR_L, select the address for writing the characters;
   ({SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} Used to select the word address)
4. Configure SPROG_DATA (high 8 bits);
5. Configure SPROG_DATA (low 8 bits)
6. Configure SPROG_CMD = 0x69;
7. Write 4 NOP instructions;
8. Start burn writing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after erasing is completed;
9. Need to continue writing data, jump to step 3;
10. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings;

Note:

1. It is recommended to repeat steps 6 and 7 once to enhance data writing stability.
2. When burn writing words, 1Word (2Bytes) is programmed each time. When using word programming in order of Address, {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]}Address increases by 2 each time it jumps, and it points to the Address programmed by the next word.
3. During word programming, the data (SPROG_DATA) should be configured twice in succession.The first configuration data is high 8 bits, and the second configuration data is low 8 bits. If the data is configured multiple times in a row, the last programmed data is the combination of the first configured data and the last configured data. At this time, the first configured data is high 8 bits, and the last configured data is low 8 bits.

16.6. Address Correspondence

Block	Sector	Page	Logical address			Physical address (HEX)
			Address(DEC)	SPROG_ADDR_H [1:0] (HEX)	SPROG_ADDR_L [7:0] (HEX)	
0	0	0	0	00	00	8000
0	0	0	1	00	01	8001
0	0	0	2	00	02	8002
0	0	0	3	00	03	8003
…	…	…	…	…	…	…
0	0	0	124	00	7C	807C
0	0	0	125	00	7D	807D
0	0	0	126	00	7E	807E
0	0	0	127	00	7F	807F
0	0	1	128	00	80	8080
0	0	1	129	00	81	8081
0	0	1	130	00	82	8082
0	0	1	131	00	83	8083
…	…	…	…	…	…	…
0	0	1	252	00	FC	80FC
0	0	1	253	00	FD	80FD
0	0	1	254	00	FE	80FE
0	0	1	255	00	FF	80FF
0	0	2	256	01	0	8100
0	0	2	257	01	1	8101
0	0	2	258	01	2	8102
0	0	2	259	01	3	8103
…	…	…	…	…	…	…
0	0	2	380	01	7C	817C
0	0	2	381	01	7D	817D
0	0	2	382	01	7E	817E
0	0	2	383	01	7F	817F
0	0	3	384	01	80	8180
0	0	3	385	01	81	8181
0	0	3	386	01	82	8182
0	0	3	387	01	83	8183
…	…	…	…	…	…	…
0	0	3	508	01	FC	81FC
0	0	3	509	01	FD	81FD
0	0	3	510	01	FE	81FE

0	0	3	511	01	FF	81FF
0	1	4	512	02	00	8200
0	1	4	513	02	01	8201
0	1	4	514	02	02	8202
0	1	4	515	02	03	8203
…	…	…	…	…	…	…
0	1	4	636	02	7C	827C
0	1	4	637	02	7D	827D
0	1	4	638	02	7E	827E
0	1	4	639	02	7F	827F
0	1	5	640	02	80	8280
0	1	5	641	02	81	8281
0	1	5	642	02	82	8282
0	1	5	643	02	83	8283
…	…	…	…	…	…	…
0	1	5	764	02	FC	82FC
0	1	5	765	02	FD	82FD
0	1	5	766	02	FE	82FE
0	1	5	767	02	FF	82FF
0	1	6	768	03	00	8300
0	1	6	769	03	01	8301
0	1	6	770	03	02	8302
0	1	6	771	03	03	8303
…	…	…	…	…	…	…
0	1	6	892	03	7C	837C
0	1	6	893	03	7D	837D
0	1	6	894	03	7E	837E
0	1	6	895	03	7F	837F
0	1	7	896	03	80	8380
0	1	7	897	03	81	8381
0	1	7	898	03	82	8382
0	1	7	899	03	83	8383
…	…	…	…	…	…	…
0	1	7	1020	03	FC	83FC
0	1	7	1021	03	FD	83FD
0	1	7	1022	03	FE	83FE
0	1	7	1023	03	FF	83FF

Logical adress and physical address correspondence Table

16.7. Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xF9	SPROG_ADDR_H	RW	0x00_0000b	Address control register
0xFA	SPROG_ADDR_L	RW	0000_0000b	Address register low 8 bits
0xFB	SPROG_DATA	RW	0000_0000b	Data register
0xFC	SPROG_CMD	RW	0000_0000b	Command configuration register
0xFD	SPROG_TIM	RW	1001_1010b	Erase time control register

16.7.1. Address Control Register

SPROG_ADDR_H (F9H) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	**In non-BOOT upgrade mode:** Bit[7]: 0: Points to the DATA area address; 1: Reserved Bit[1:0] : The upper 2 bits of the address in the DATA area, { SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} indicates the DATA area address Bit[6:2]: Reserved **In BOOT upgrade mode:** Bit[6]: Reserved Bit[7]: Select address to enable 0: Points to the DATA area address, {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]}; 1: Point to address 0x0000~0x3FFF, {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]}

16.7.2. Address Control Register Low 8 bits

SPROG_ADDR_L (FAH) Address register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	Low 8 bits of address

16.7.3. Data Register

SPROG_DATA (FBH) Data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Data to be written

16.7.4. Command Configuration Register

SPROG_CMD (FCH) Command configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x94: DATA area block erase; Write 0x95: DATA area sector erase; Write 0x96: DATA area page erase; Write 0x69: DATA area word write; When data 0x12, 0x34, 0x56, 0x78, and 0x9A are continuously written, the BOOT upgrade mode is entered When data 0xfe, 0xDC, 0xBA, 0x98, and 0x76 are continuously written, the BOOT upgrade mode is exited If CFG_BOOT_EN=1 or the program is running in a non-boot space, the BOOT upgrade mode cannot be entered

16.7.5. Erase Time Control Register

SPROG_TIM (FDH) Erase time control register

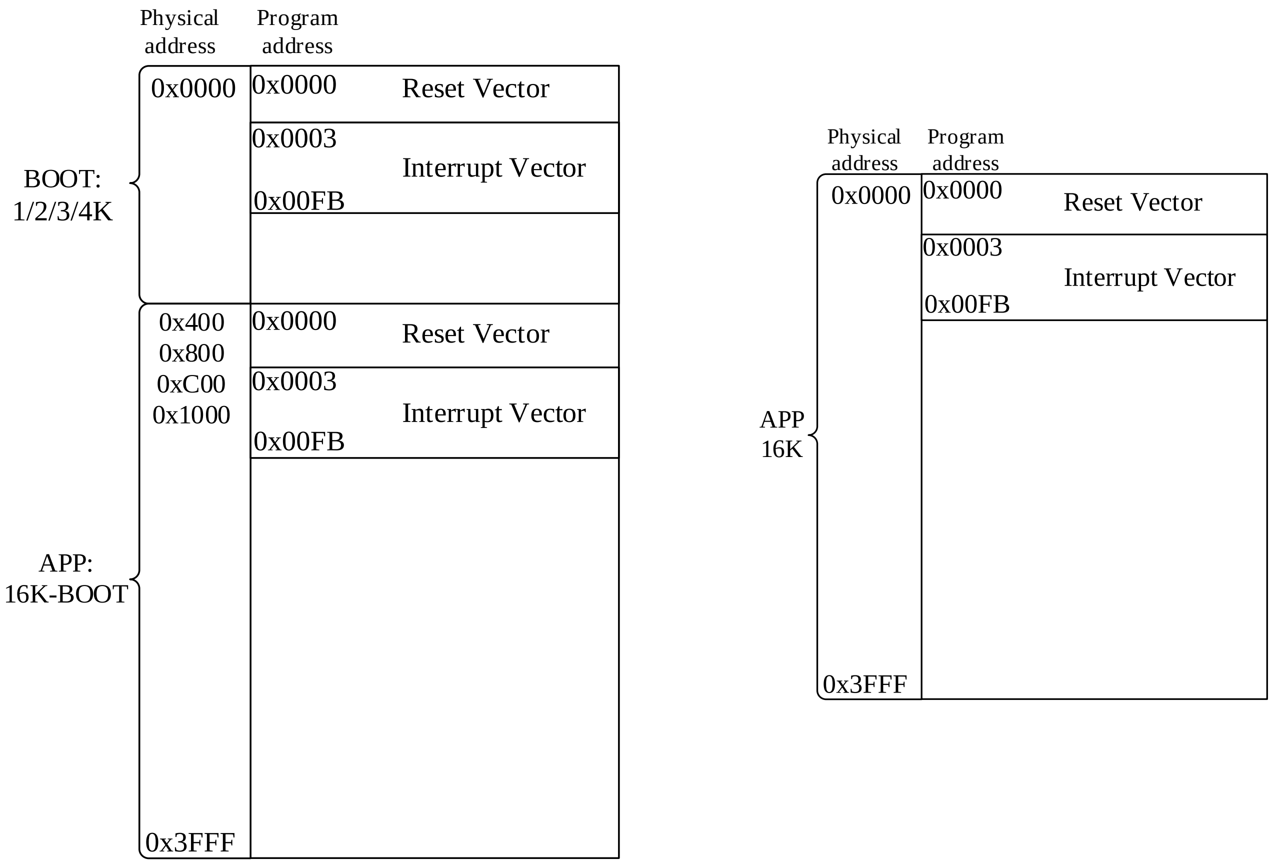
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	1	1	0	1	0

Bit number	Bit symbol	Description
7~5	SPROG_TIM[7:5]	Word write time configuration register 000: Word write time = 113.1μs, (word burn step 6 and 7) Others: Reserved;
4~0	SPROG_TIM[4:0]	The erase time is set to SPROG_TIM[4:0]=0~31 **In non-boot upgrade mode:** When SPROG_TIM[4:0] = 0~1, reserved. When SPROG_TIM[4:0] = 2~25, DATA area erasure time = {1+2* SPROG_TIM[4:0]}+0.01 (ms) When SPROG_TIM[4:0] = 26~31. DATA area erasure time = 10.01 (ms) **When operating the main block in Boot upgrade mode:** When SPROG_TIM[4:0] = 0~25. CODE area erasure time = 20.01+5* SPROG_TIM[4:0] (ms) When SPROG_TIM[4:0] = 26~31. CODE area erasure time = 100.01 (ms)

17. IAP Operation

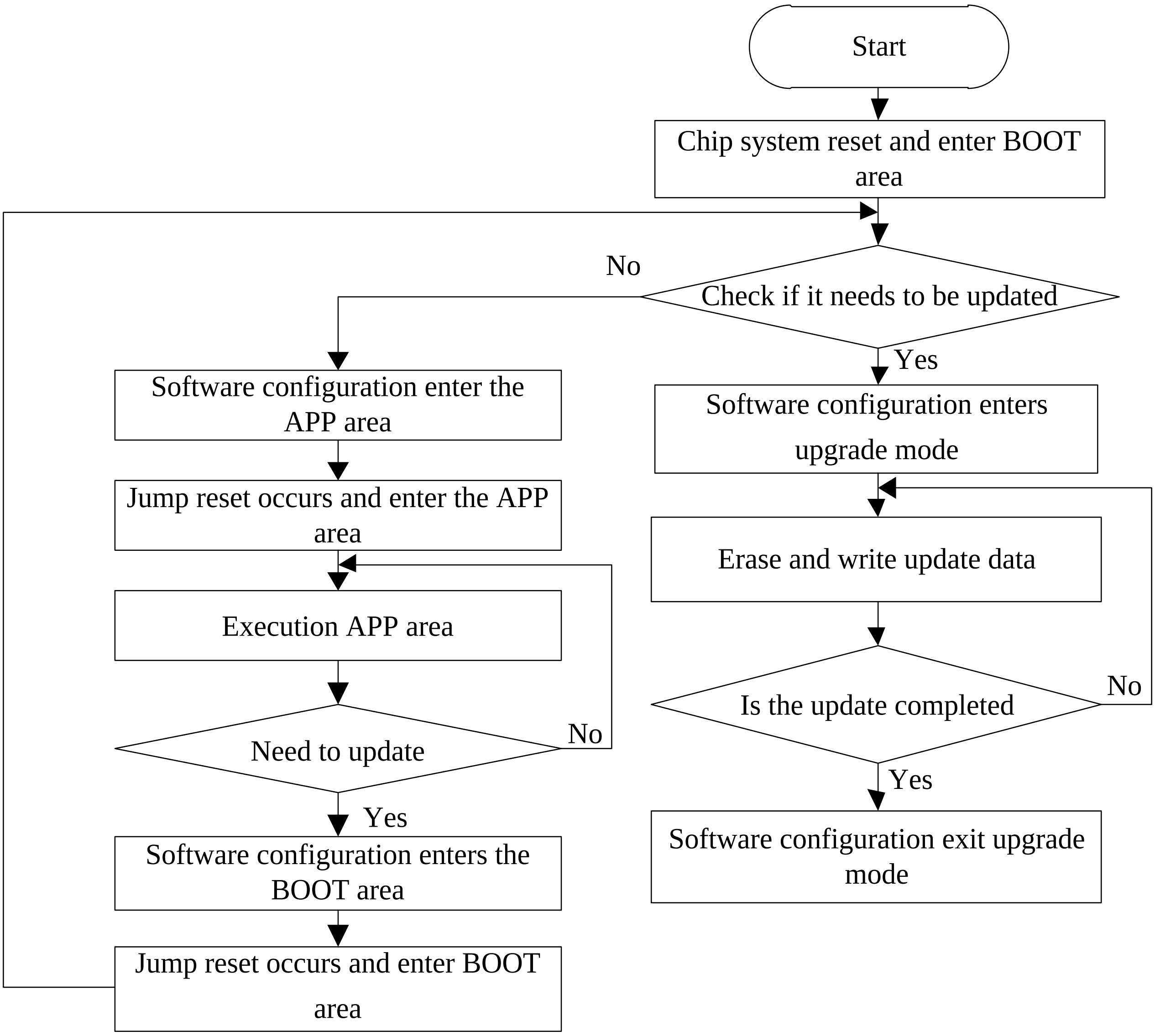
17.1. Function Overview

The BF7612DMXX-SJLX supports IAP BOOT upgrade function, the size of BOOT area is 1/2/3/4K. The jump between the BOOT area and the APP area is realized by sending the IAP operation command. BOOT has its own storage write protection. The size of the BOOT area is selected by the configuration word CFG_31: [1:0]-CFG_BOOT_SEL: 0: 1K, 1: 2K, 2: 3K, 3: 4K. BOOT function enables by configuration word CFG_31:[2]-CFG_BOOT_EN selection: 0: Open BOOT function; 1: Close BOOT function.



Left: BOOT and APP partition map; Right: APP map, not-BOOT map

17.2. IAP Operating Procedure



IAP operation flowchart

17.2.1. IAP Erase Steps

In BOOT upgrade mode:

1. SPROG_TIM[4:0] = 0~25 (suggest 100ms), configure SPROG_TIM[7:5] = 0, and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_L = 0x00, SPROG_ADDR_H [7] = 1;
4. Configure {SPROG_ADDR_H [5:0], SPROG_ADDR_H [7]}, select the page 0 ~ 127 (each page 128Bytes);
5. Configure SPROG_CMD = 0x95;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after erasing is completed;
8. Need to continue erasing data, jump to step 3;
9. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings.

17.2.2. IAP Word Burn Write Steps

In BOOT upgrade mode:

1. SPROG_TIM[4:0] = 0~25 (suggest 100ms), configure SPROG_TIM[7:5] = 0, and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_H, SPROG_ADDR_L, select the burned address; ({SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]} use for select the burned address);
4. Configure SPROG_DATA (high 8 bits);
5. Configure SPROG_DATA (low 8 bits);
6. Configure SPROG_CMD = 0x69;
7. Write 4 NOP instructions;
8. Start burn writing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after completion;
9. Need to continue writing data, jump to step 3;
10. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings;

Note:

1. **It is recommended to repeat steps 6 and 7 once to enhance data writing stability.**
2. **When burn writing words, write 1Word (2 Bytes) each time. When using word programming in order of address, {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]}address increases by 2 each time it jumps, and it points to the address programmed by the next word.**
3. **During word programming, the data (SPROG_DATA) should be configured twice in succession. The first configuration data is high 8 bits, and the second configuration data is**

low 8 bits. If the data is configured multiple times in a row, the last programmed data is the combination of the first configured data and the last configured data. At this time, the first configured data is high 8 bits, and the last configured data is low 8 bits.

17.2.3. IAP Operation Instruction

Instruction	Instruction response status	Instruction data
Enter upgrade mode instruction	BOOT_EN = 1	0x12, 0x34, 0x56, 0x78, 0x9a
Exit upgrade mode instruction	BOOT_EN = 0	0xfe, 0xdc, 0xba, 0x98, 0x76
Enter APP area instruction	ROM_OFFSETH/L	0xff, 0x00, 0x88, 0x55, 0xaa
Enter BOOT area instruction	ROM_OFFSETH/L	0x37, 0xc8, 0x42, 0x9a, 0x65

Instructions for operation:

1. Enter upgrade mode instruction: SPROG_CMD sequential write: 0x12. 0x34. 0x56, 0x78, 0x9A;
2. Exit upgrade mode instruction: SPROG_CMD sequential write: 0xFE, 0xDC, 0xBA, 0x98, 0x76;
3. Enter the APP area instruction: BOOT_CMD sequential write: 0xFF, 0x00, 0x88, 0x55, 0xAA;
4. Enter the BOOT area instruction: BOOT_CMD sequential write: 0x37, 0xC8, 0x42. 0x9A, 0x65;

Instructions response status:

BOOT_EN = 1: Indicates that the BOOT upgrade mode has been entered,

BOOT_EN = 0: Indicates that the BOOT upgrade mode has been exited

ROM_OFFSETH/L address offset state: ROM_OFFSETH/L = 0x400;

ROM_OFFSETH/L address offset state: ROM_OFFSETH/L = 0x800;

ROM_OFFSETH/L address offset state: ROM_OFFSETH/L = 0xC00;

ROM_OFFSETH/L address offset state: ROM_OFFSETH/L = 0x1000;

If currently in the boot area: ROM_OFFSETH/L = 0x0000.

Physical address of program execution address = PC + ROM_OFFSETH/L.

Notes:

1. When writing SPROG_CMD, BOOT_CMD instruction data, it must be written in order, otherwise it needs to be written again.
2. The working voltage of MCU is 2.7V~5.5V, and the MCU may work abnormally at 1.5V~2.7V, resulting in abnormal update and misoperation. Therefore, it is recommended not to perform IAP operation when the ADC or LVDT detection voltage is lower than 2.7V before IAP operation.
3. It is recommended to shield the interrupt during the update process to ensure that the IAP operation will not be affected by the interruption, and resume the interruption after the IAP operation is completed, and perform data verification after updating the data to ensure that the data is updated correctly.

17.2.4. Address Correspondence in BOOT Upgrade Mode

SPROG_ADDR_H[5:1]	Block	Byte write physical address corresponding range (HEX)		
2	2	00000400	--->	000005FF
3	3	00000600	--->	000007FF
4	4	00000800	--->	000009FF
5	5	00000A00	--->	00000BFF
6	6	00000C00	--->	00000DFF
7	7	00000E00	--->	00000FFF
8	8	00001000	--->	000011FF
9	9	00001200	--->	000013FF
10	10	00001400	--->	000015FF
11	11	00001600	--->	000017FF
12	12	00001800	--->	000019FF
13	13	00001A00	--->	00001BFF
14	14	00001C00	--->	00001DFF
15	15	00001E00	--->	00001FFF
16	16	00002000	--->	000021FF
17	17	00002200	--->	000023FF
18	18	00002400	--->	000025FF
19	19	00002600	--->	000027FF
20	20	00002800	--->	000029FF
21	21	00002A00	--->	00002BFF
22	22	00002C00	--->	00002DFF
23	23	00002E00	--->	00002FFF
24	24	00003000	--->	000031FF
25	25	00003200	--->	000033FF
26	26	00003400	--->	000035FF
27	27	00003600	--->	000037FF
28	28	00003800	--->	000039FF
29	29	00003A00	--->	00003BFF
30	30	00003C00	--->	00003DFF
31	31	00003E00	--->	00003FFF

Note:

1. Word write physical address corresponding register: {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]};
2. 512Bytes per block;

3. When operating the BOOT area, BOOT is write protected and the operation is invalid.
4. When the BOOT function is used, the absolute address of all CODE areas of the program needs to be subtracted from the offset address of ROM_OFFSET_H/L (PC - ROM_OFFSET), and then the absolute address of the CODE area is accessed.

17.3. Registers

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xF9	SPROG_ADDR_H	RW	0x00_0000b	Address control register
0xFA	SPROG_ADDR_L	RW	0000_0000b	Address register low 8 bits
0xFB	SPROG_DATA	RW	0000_0000b	Data register
0xFC	SPROG_CMD	RW	0000_0000b	Command configuration register
0xFD	SPROG_TIM	RW	1001_1010b	Erase time control register

Secondary bus register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x21	BOOT_CMD	RW	0000_0000b	Program space jump instruction register
0x22	ROM_OFFSET_L	R	0000_0000b	Address offset of the CODE field low 8 bits
0x23	ROM_OFFSET_H	R	0000_0000b	Address offset of the CODE field high 8 bits
0x24	BOOT_EN	R	xxxx_xxx0b	BOOT mode status register

Note: In BOOT upgrade mode, registers SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused for BOOT upgrade function

17.3.1. Address Control Register

SPROG_ADDR_H (F9H) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	**In non-BOOT upgrade mode:** Bit[6:2]: Reserved Bit[7]0: Points to the DATA area address; 1: Reserved Bit[1:0]: The upper 2 bits of the address in the DATA area, { SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} indicates the DATA area address **In BOOT upgrade mode:**

		Bit[6]: Reserved Bit[7]: Select address to enable 0: Points to the DATA area address, {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]}; 1: Point to address 0x0000~0x3FFF, {SPROG_ADDR_H[5:0], SPROG_ADDR_L[7:0]}

17.3.2. Address Control Register Low 8 bits

SPROG_ADDR_L (FAH) Address control register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	Low 8 bits of address

17.3.3. Data Register

SPROG_DATA (FBH) Data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Data to be written

17.3.4. Command Configuration Register

SPROG_CMD (FCH) Command configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	When data 0x12, 0x34, 0x56, 0x78, and 0x9A are continuously written, the BOOT upgrade mode is entered When data 0xfe, 0xDC, 0xBA, 0x98, and 0x76 are

		continuously written, the BOOT upgrade mode is exited If CFG_BOOT_EN=1 or the program is running in a non-boot space, the BOOT upgrade mode cannot be entered

17.3.5. Erase Time Control Register

SPROG_TIM (FDH) Erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	1	1	0	1	0

Bit number	Bit symbol	Description
7~5	SPROG_TIM[7:5]	Word write time configuration register 000: Word write time = 113.1μs, (word burn step 6 and 7) Others: Reserved;
4~0	SPROG_TIM[4:0]	The erase time is set to SPROG_TIM[4:0]=0~31 **In non-boot upgrade mode:** When SPROG_TIM[4:0] = 0~1, reserved When SPROG_TIM[4:0] = 2~25. DATA area erasure time = {1+2* SPROG_TIM[4:0]}+0.01 (ms) When SPROG_TIM[4:0] = 26~31. DATA area erasure time = 10.01 (ms) **When operating the main block in Boot upgrade mode:** When SPROG_TIM[4:0] = 0~25. CODE area erasure time = 20.01+5* SPROG_TIM[4:0] (ms) When SPROG_TIM[4:0] = 26~31. CODE area erasure time = 100.01 (ms)

17.4. Secondary Bus Registers

17.4.1. Program Space Jump Instruction Register

BOOT_CMD (21H) Program space jump instruction register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_CMD[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	BOOT_CMD[7:0]	Configure the program space jump instruction, Write 5 consecutive groups of data into the main program space: 0xff, 0x00, 0x88, 0x55, 0xaa Write five groups of data to boot: 0x37, 0xc8, 0x42, 0x9a, 0x65 The value read out is the byte written recently

17.4.2. Address Offset of the CODE Field

ROM_OFFSET_L (22H) Address offset of the CODE field low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	The address offset of the CODE field(low 8 bits)

ROM_OFFSET_H (23H) Address offset of the CODE field high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	The address offset of the CODE field(high 8 bits)

17.4.3. BOOT Mode Status Register

BOOT_EN (24H) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	BOOT_EN
R/W	-	-	-	-	-	-	-	R
Reset value	-	-	-	-	-	-	-	0

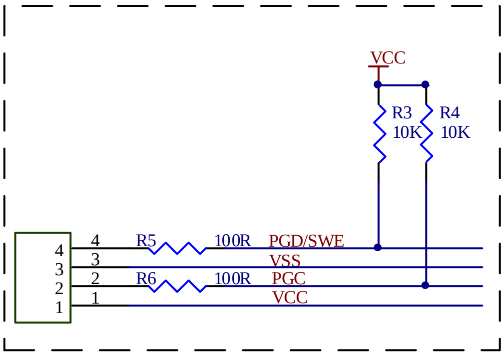
Bit number	Bit symbol	Description
0	BOOT_EN	1: Indicates that the BOOT upgrade mode has been entered, 0: Indicates that the BOOT upgrade mode has been exited. Note: In BOOT upgrade mode, SPROG_ADDR_H,

		SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as BOOT upgrade function.

18. Burning and Debugging

18.1. SWE Circuit Connection

Two-wire programming and single-wire debugging. When performing simulation debugging, you need to connect a SWE wire. In the SWE debugging mode, the IO function of the SWE port is blocked. It is recommended not to configure other functions of the SWE debugging IO port to avoid affecting the SWE debugging function.



SWE circuit connection reference diagram

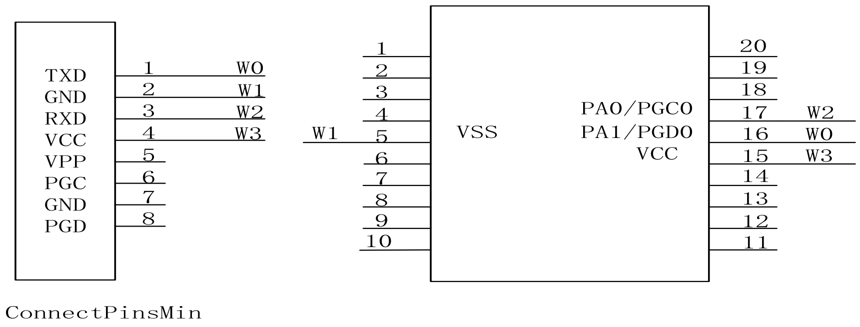
18.2. Touch Key Data-assisted Programming and Debugging

Connect the chip PGC0(PGC1/PGC2), PGD0(PGD1/PGD2), VCC, VSS four lines. When entering the programming interface, select the chip of the corresponding model. Open the compiled HEX file, click on a built-in flash to wait for burning.

When entering the debugging interface, first burn the HEX file with the debugging data sending mode, and click Start debugging to view the key data.

Note:

Refer to the TK recording debugging guide for specific operation Description.



BF7612DM20-SJLX burning wiring diagram

19. CPU Instruction System

19.1. Instruction Code

The BF7612DMXX-SJLX instructions are divided into signal-byte instructions, double-byte instructions and three-byte instructions.

Signal-byte instructions: A signal-byte instruction consists of 8 bit binary code. There are only instruction opcodes in the instruction, no instruction operand or instruction operand is implied in the instruction opcode. There are 49 such instructions.

Double-byte instructions: Consists of two bytes, one for opcode and the other for the operand (or operand address), stored in order in program memory. There are 46 such instructions.

Three-byte instructions: Consists of one byte of instruction opcode and two bytes of operands (or operand address). There are 16 such instructions.

19.2. Instruction Set

In order to describe the instructions conveniently, some symbols are used in the instructions. The meanings of these symbols are as follows:

Addr 11	Low 11 bit address
addr 16	16 bit address
direct	Direct addressing, 8 bit internal data and address(including SFR)
bit	Bit address
#data	8 bit immediate
#data16	16 bit immediate
rel	Signed 8 bit relative displacement
n	Number 0~7
Rn	R0~R7 working register of the current register bank
i	Number 0, 1
Ri	working register R0, R1
@	Register indirect addressing
←	Data transfer direction
∧	Logic 'and'
∨	Logic 'or'
⊕	Logic 'xor'
√	Have an effect on the flag
×	No effect on the flag

CPU instruction symbol table

Provides the assembly instructions used, the function of each instruction, the number of bytes occupied, the execution cycle of the instruction, and the effect on the corresponding flags:

8 bit data transfer instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV A	Rn	A←(Rn)	√	×	×	×	1	1
	direct	A←(direct)	√	×	×	×	2	1
	@Ri	A←((Ri))	√	×	×	×	1	1
	#data	A←data	√	×	×	×	2	1
MOV Rn	A	Rn←(A)	×	×	×	×	1	1
	direct	Rn←(direct)	×	×	×	×	2	2
	#data	Rn←data	×	×	×	×	2	1
MOV direct1	A	direct1←(A)	×	×	×	×	2	1
	Rn	direct1←(Rn)	×	×	×	×	2	1
	direct2	direct1←(direct2)	×	×	×	×	3	2
MOV direct	@Ri	direct←((Ri))	×	×	×	×	2	2

	#data	direct←data	×	×	×	×	3	1
MOV @Ri	A	(Ri)←(A)	×	×	×	×	1	1
	direct	(Ri)←(direct)	×	×	×	×	2	2
	#data	(Ri)←data	×	×	×	×	2	1
16 bit data transfer instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV DPTR,#data16		DPTR←data16		×	×	×	3	1
External data transfer and table lookup instructions								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOVX @DPTR,A		(DPTR)←(A)	×	×	×	×	1	1
MOVC A,	@A+DPTR	A←((A)+(DPTR))	√	×	×	×	1	1
	@A+PC	A←((A)+(PC))	√	×	×	×	1	1
MOVX A,	@DPTR	A←(DPTR)	√	×	×	×	1	1
Notes: The number of cycles and the number of bytes of the MOVX instruction can be configured through registers CKCON<2:0>.								
Exchange class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
XCH A,	Rn	(Rn)←(A)	√	×	×	×	1	1
	direct	(A)←(direct)	√	×	×	×	2	2
	@Ri	(A)←((Ri))	×	×	×	×	1	2
XCHD A,@Ri		(A)3~0~((Ri))3~0	√	×	×	×	1	2
SWAP A		(A)7-4~(A)3-0	√	×	×	×	1	1
Arithmetic operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
ADD A,	Rn	A←(A)+(Rn)	√	√	√	√	1	1
	direct	A←(A)+(direct)	√	√	√	√	2	2
	@Ri	A←(A)+((Ri))	√	√	√	√	1	2
	#data	A←(A)+data	√	√	√	√	2	1
ADDC A,	Rn	A←(A)+(Rn)+(C)	√	√	√	√	1	1
	direct	A←(A)+(direct) +(C)	√	√	√	√	2	2
	@Ri	A←(A)+((Ri)) +(C)	√	√	√	√	1	2
	#data	A←(A)+data+(C)	√	√	√	√	2	1

INC	A	A←(A)+1	√	×	×	×	1	1
	Rn	Rn←(Rn)+1	×	×	×	×	1	1
	direct	direct←(direct)+1	×	×	×	×	2	2
	@Ri	(Ri)←((Ri))+1	×	×	×	×	1	2
	DPTR	DPTR←((DPTR))+1	×	×	×	×	1	1
DA A		BCD code adjustment	√	×	√	√	1	1
SUBB A	Rn	A←(A)-(Rn)-(C)	√	×	×	×	1	1
	direct	A←(A)-(direct)-(C)	√	√	√	√	2	2
	@Ri	(A)←(A)-((Ri))-(C)	√	√	√	√	1	2
	#data	A←(A)-data-(C)	√	√	√	√	2	1
DEC	A	A←(A)-1	√	×	×	×	1	1
	Rn	Rn←(Rn)-1	×	×	×	×	1	1
	direct	direct←(direct)-1	×	×	×	×	2	2
	@Ri	(Ri)←((Ri))-1	×	×	×	×	1	2
MUL AB		BA←(A)*(B) after performing the multiplication operation, the lower byte is stored in A and the high byte is stored in B.	√	√	×	0	1	1
DIV AB		A←(A)/(B) B←remainder	√	√	×	0	1	1

Notes: When the DA instruction is used, the adjustment rules are as follows: if the low 4 bits of accumulator A are greater than 9 or AC=1. then A←A+06H; if the high 4 bits of accumulator A are greater than 9 or CY=1. then A←A+60H.

Logical operation instruction

Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
CLR A		A←00H	√	×	×	×	1	1
CPL A		A←($\overline{A}$)	√	×	×	×	1	1
ANL A,	Rn	A←(A)∧(Rn)	√	×	×	×	1	1
	direct	A←(A)∧(direct)	√	×	×	×	2	2
	@Ri	A←(A)∧((Ri))	√	×	×	×	1	2
	#data	A←(A)∧data	√	×	×	×	2	1
ANL direct,	A	direct←(A)∧(direct)	×	×	×	×	2	2
	#data	direct←(direct)∧	×	×	×	×	3	2

		data						
ORL A,	Rn	A←(A)∨(Rn)	√	×	×	×	1	1
	direct	A←(A)∨(direct)	√	×	×	×	2	2
	@Ri	A←(A)∨((Ri))	√	×	×	×	1	2
	#data	A←(A)∨data	√	×	×	×	2	1
ORL direct,	A	direct←(direct)∨(A)	×	×	×	×	2	2
	#data	direct←(direct)∨data	×	×	×	×	3	2
XRL A,	Rn	A←(A)⊕(Rn)	√	×	×	×	1	1
	direct	A←(A)⊕(direct)	√	×	×	×	2	2
	@Ri	A←(A)⊕((Ri))	√	×	×	×	1	2
	#data	A←(A)⊕data	√	×	×	×	2	1
XRL direct,	A	direct←(direct)⊕(A)	×	×	×	×	2	2
	#data	direct←(direct)⊕data	×	×	×	×	3	2

Loop, shift class instruction							
Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
RL A	The content in A is rotated left by one bit.	×	×	×	×	1	1
RLC A	A content with carry left shift one bit.	√	×	×	√	1	1
RR A	The content in A is rotated right by one bit.	×	×	×	×	1	1
RRC A	A content with carry right shift one bit.	√	×	×	√	1	1

Call, return class instruction							
Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
LCALL addr16	(PC)←(PC)+3. (SP)←(PC), (PC)←addr16	×	×	×	×	3	2
ACALL addr11	(PC)←(PC)+2. (SP)←(PC), (PC10~0)←addr11	×	×	×	×	2	2
RET	(PC)←((SP))	×	×	×	×	1	2

RETI	(PC)←((SP)) return from interrupt	×	×	×	×	1	2
Transfer class instruction							
Mnemonic	function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
LJMP addr16	PC←addr15~0	×	×	×	×	3	1
AJMP addr11	PC10~0←addr10~0	×	×	×	×	2	1
SJMP rel	PC←(PC)+rel	×	×	×	×	2	1
JMP @A+DPTR	PC←(A)+(DPTR)	×	×	×	×	1	1
JZ rel	PC←(PC)+2. If (A)=0, PC←(PC)+rel	×	×	×	×	2	2
JNZ rel	PC←(PC)+2. If (A)≠0, PC←(PC)+rel	×	×	×	×	2	2
JC rel	PC←(PC)+2. If (CY)=1. PC←(PC)+rel	×	×	×	×	2	2
JNC rel	PC←(PC)+2. If (CY)=0,PC←(PC)+rel	×	×	×	×	2	2
JB bit,rel	PC←(PC)+3. If (bit)=1. PC←(PC)+rel	×	×	×	×	3	2
JNB bit,rel	PC←(PC)+3. If (bit)=0,PC←(PC)+rel	×	×	×	×	3	2
JBCbit,rel	PC←(PC)+3. If (bit)=1. bit←0, PC←(PC)+rel	×	×	×	×	3	2

CJNE A, direct,rel	PC←(PC)+3.
	If (A) ≠direct
	PC(PC)+rel
	If (A)<(direct),
	CY←1
		×	×	×	×	3	2

A,#data,rel	PC←(PC)+3. If (A) ≠data PC(PC)+rel	×	×	×	×	3	2

		If (A)<(data), CY←1						

	Rn,#data,rel	PC←(PC)+3.
		If (Rn) ≠data
		PC←(PC)+rel
		If (Rn)<(data),
		CY←1
			×	×	×	×	3	1

	@Ri,#data,rel	PC←(PC)+3.
		If ((Ri)) ≠data
		PC←(PC)+rel
		If ((Ri))<(data),
		CY←1
			×	×	×	×	3	2

DJNZ	Rn,rel	PC←(PC)+2. Rn←(Rn)-1. If (Rn) ≠0, PC←(PC)+rel	×	×	×	×	2	1
	direct,rel	PC←(PC)+3. (direct)←(direct)-1. If (direct) ≠0, PC←(PC)+rel	×	×	×	×	3	2
Stack, empty operation class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
PUSH direct		SP←(SP)+1.(SP)←(direct)	×	×	×	×	2	2
POP direct		direct←(SP),SP←(SP)-1	×	×	×	×	2	2
NOP		empty operation	×	×	×	×	1	1
Bit manipulation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV	C,bit	CY←bit	×	×	×	√	2	2
	bit,C	bit←CY	×	×	×	×	2	2
CLR	C	CY←0	×	×	×	√	1	1
	bit	bit←0	×	×	×	×	2	2
SETB	C	CY←1	×	×	×	√	1	1
	bit	bit←1	×	×	×	×	2	2
CPL	C	CY←($\overline{CY}$)	×	×	×	√	1	1
	bit	bit←($\overline{bit}$)	×	×	×	×	2	2
ANL	C,bit	C←(C)∧(bit)	×	×	×	√	2	2

	C ,/bit	C←(C)∧($\overline{bit}$)	×	×	×	√	2	2
ORL	C,bit	C←(C)∨(bit)	×	×	×	√	2	2
	C,/bit	C←(C)∨($\overline{bit}$)	×	×	×	√	2	2
Pseudo-instruction								
Mnemonic	Mnemonic		Mnemonic					
ORG	【tab:】 ORG addr16		Define the first address of tab					
EQU	tab EQU data/tab		Assign values to labels					
DB	【tab:】 DB item or item tabel		The byte content used to define a cell or batch of cells of memory					
DW	【tab:】 DW item or item tabel		16 bit word content used to define two or more cells in memory					
DS	【tab:】 DS expression		Specifies to leave several memory cells starting with the label					
BIT	tab BIT address		Assign a bit address to a label					
END	END is placed at the end of the assembly language program to tell the assembler that the source program ends here.							

CPU instruction set table

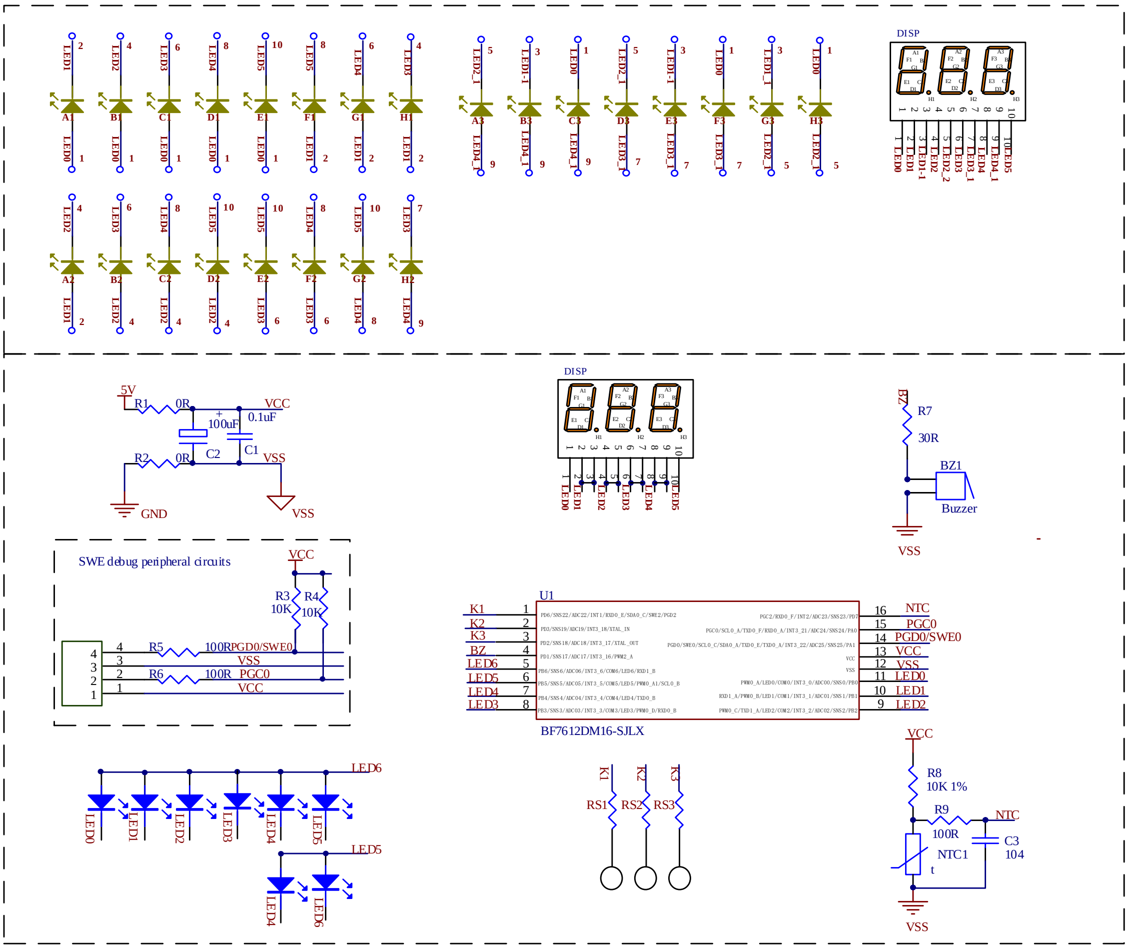
CPU related register

SFR register				
Address	Name	RW	Reset value	Description
0x81	SP	RW	0x07	Stack pointer register
0x82	DPL	RW	0x00	Data pointer register 0 low 8 bit
0x83	DPH	RW	0x00	Data pointer register 0 high 8 bit
0x87	PCON	RW	0x00	Low power mode select register
0xE0	ACC	RW	0x00	Accumulator
0xF0	B	RW	0x00	B register

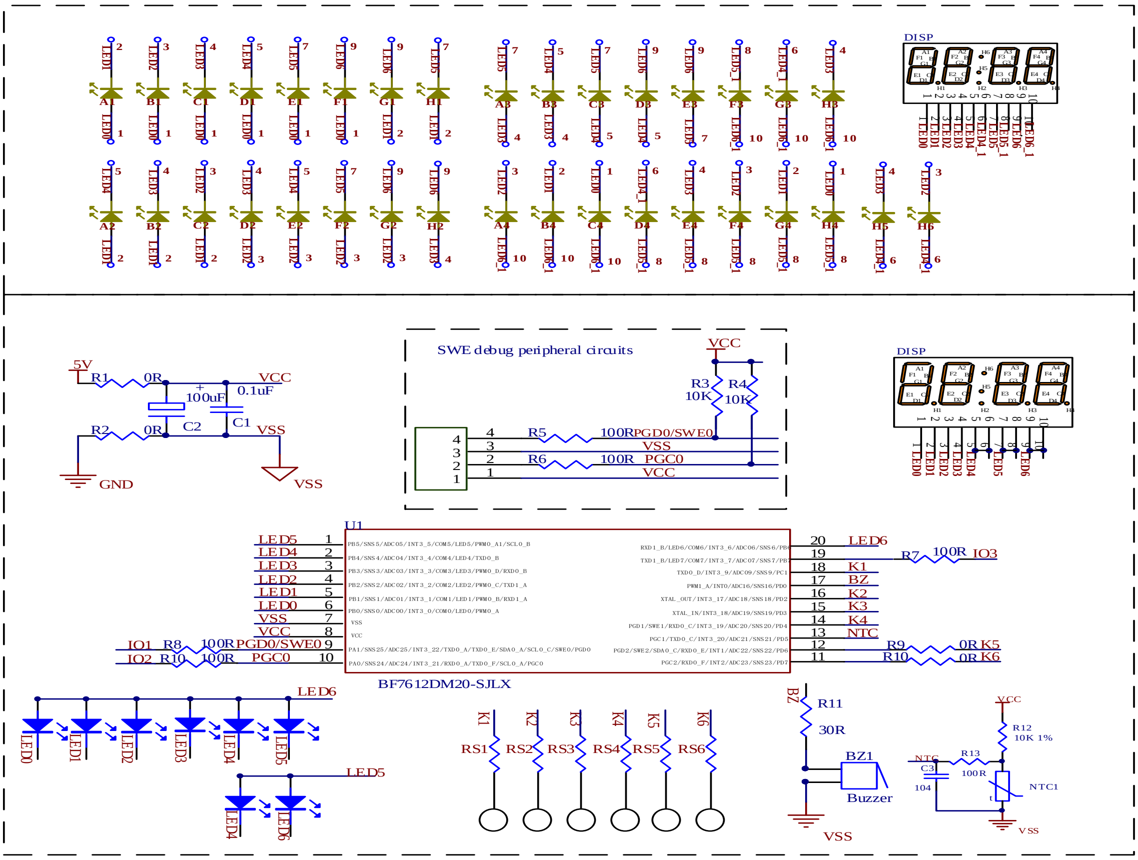
CPU SFR register list

20. Reference Application Circuits

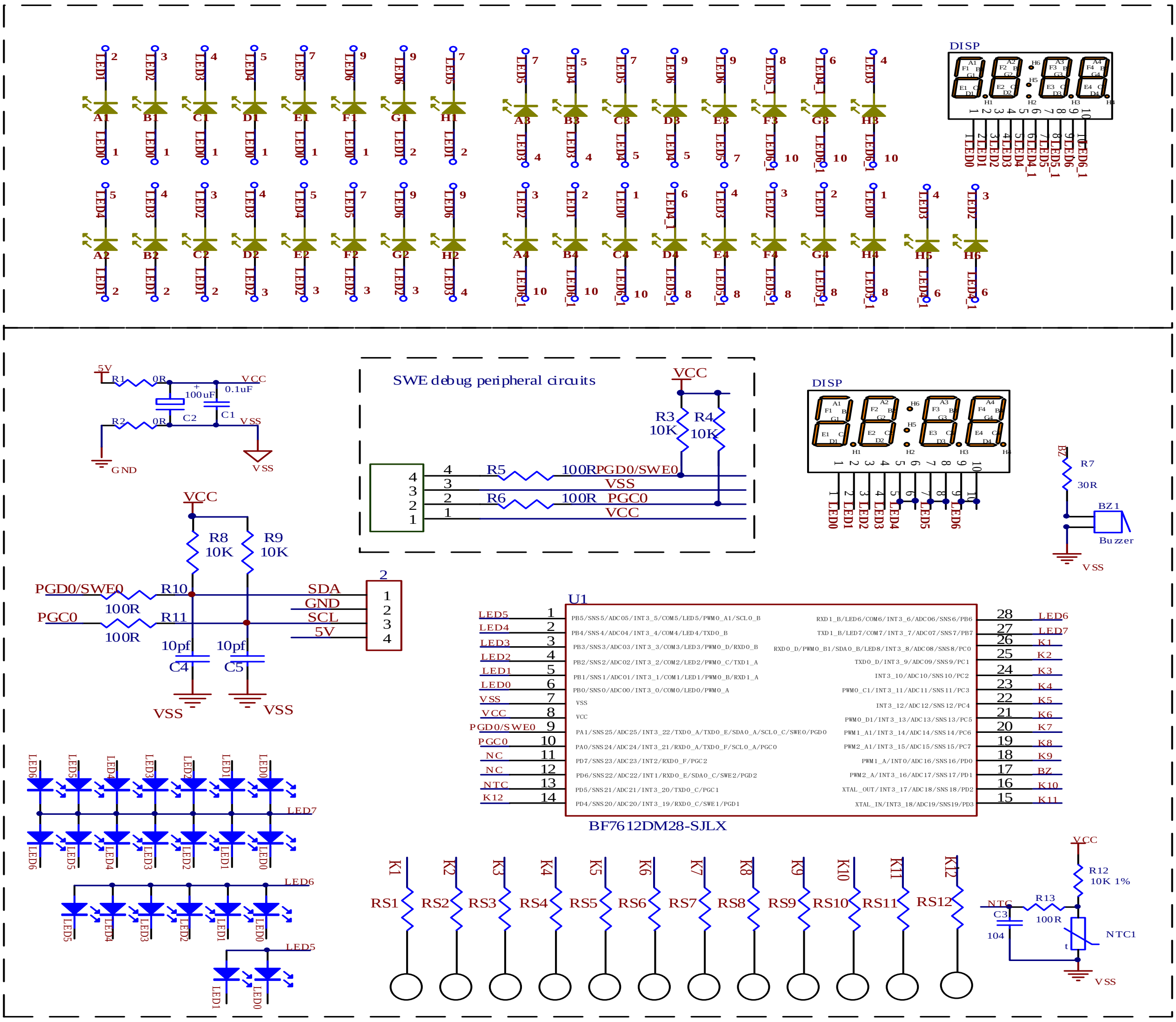
20.1. BF7612DM16-SJLX Reference Circuit



20.2. BF7612DM20-SJLX Reference Circuit



20.3. BF7612DM28-SJLX Reference Circuit

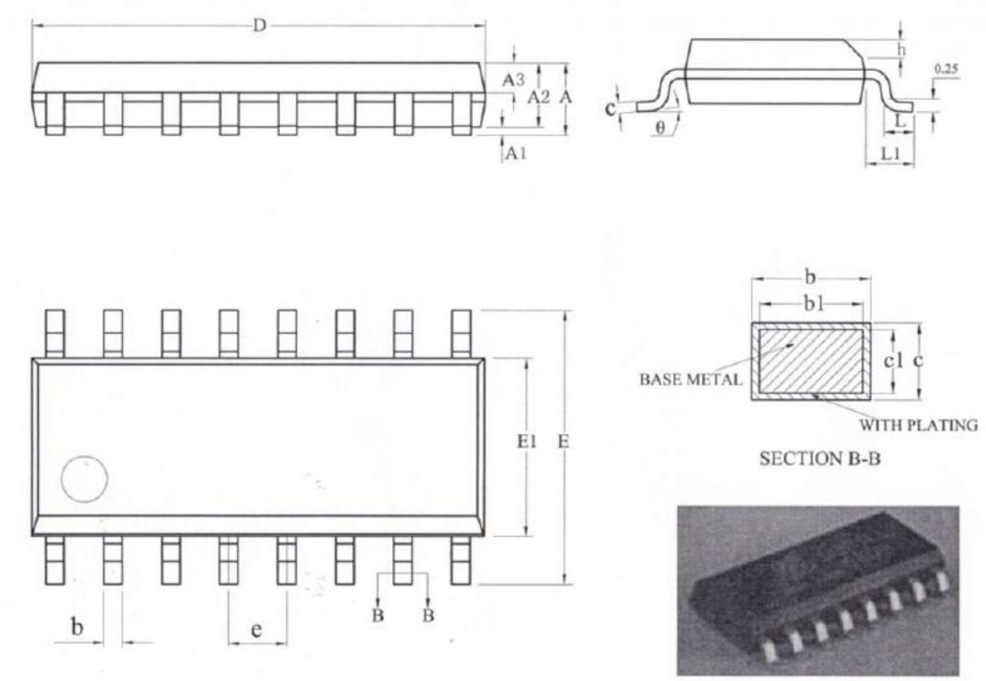


Note:

1. **The above schematic diagram is for reference only.**
2. **RSX channel resistance recommended 1k~8.2k, conventional 4.7k.**
3. **The SWE debugging peripheral circuit is only used for SWE debugging. If there is a pull-up resistor on the emulator or adapter board, there is no need to connect the SWE pull-up resistor.**
4. **The power supply and the ground are wired in parallel, and the magnetic beads are connected in series. The EMI test item (RE) can increase the test margin. The recommended parameter is 600Ω@100MHz.**
5. **The power-on time of 0~5V is recommended to be greater than 1ms. If the power-on time is less than 1ms, it is recommended to connect a 10Ω resistor in series with the power supply, and the power supply filter capacitor should be at least 22uF.**

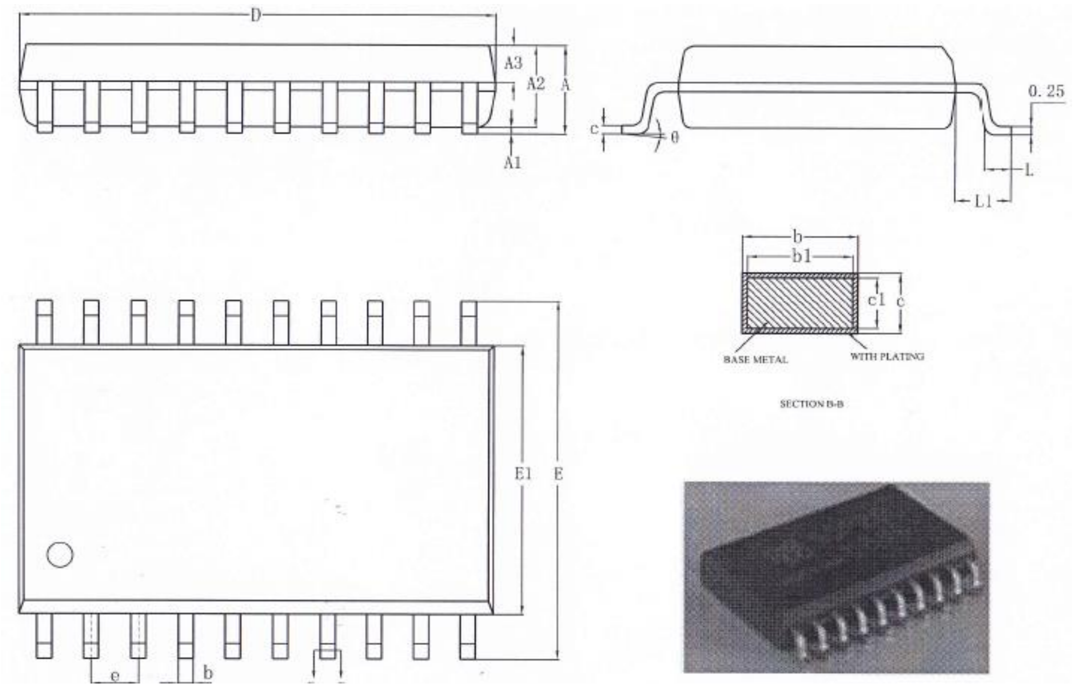
21. Packages

21.1. SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1 (1)	0.38	0.41	0.44
c (2)	0.20	—	0.25
c1	0.19	0.20	0.21
D (3)	9.80	9.90	10.00
E	5.80	6.00	6.20
E1 (4)	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

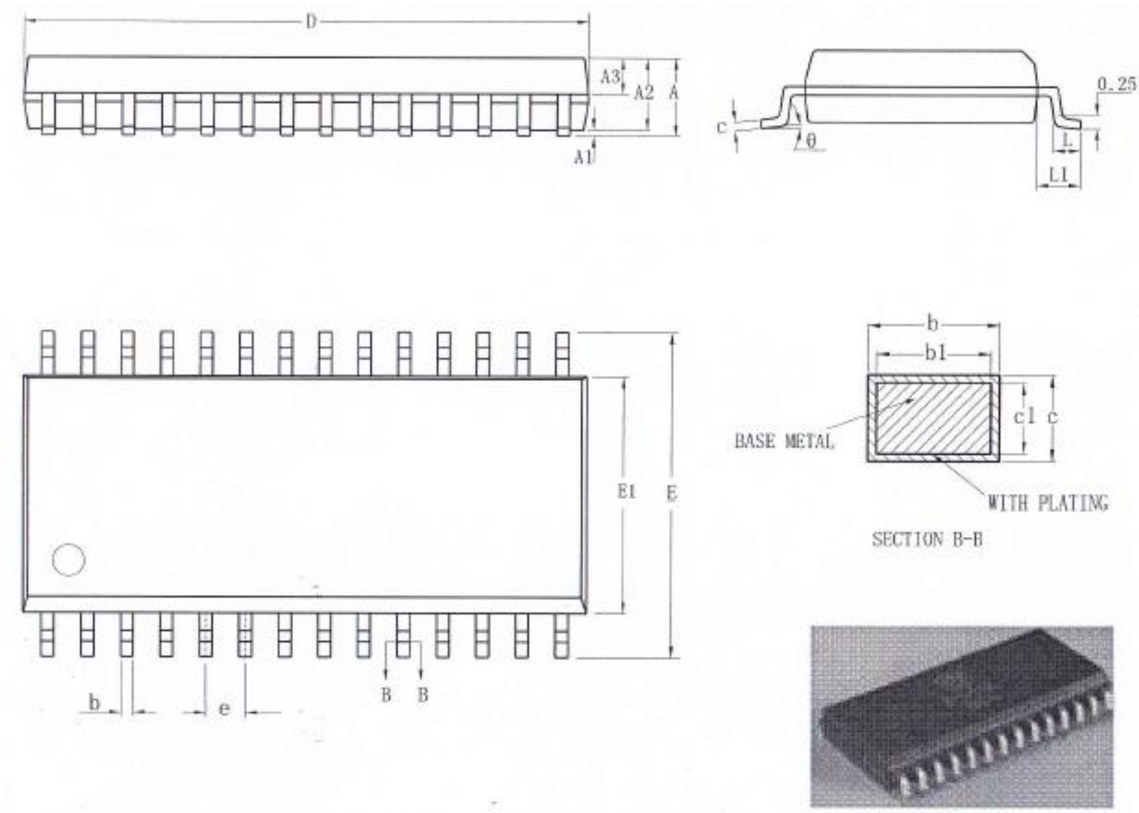
21.2. SOP20



DIM	SOP020 MILLIMETERS		
	MIN	NOM	MAX
A	-	-	2.650
A1	0.100	0.200	0.300
A2	2.250	2.300	2.350
b	0.350	-	0.440
c	0.250	-	0.310
D	12.600	12.800	13.000
E1	7.300	7.500	7.700
E	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	-	1
θ	0 °	-	8 °
Face the waste rubber	-	-	0.200
Total length of plastic sealing body	12.800	13.000	13.300

SOP20 package infographic

21.3. SOP28



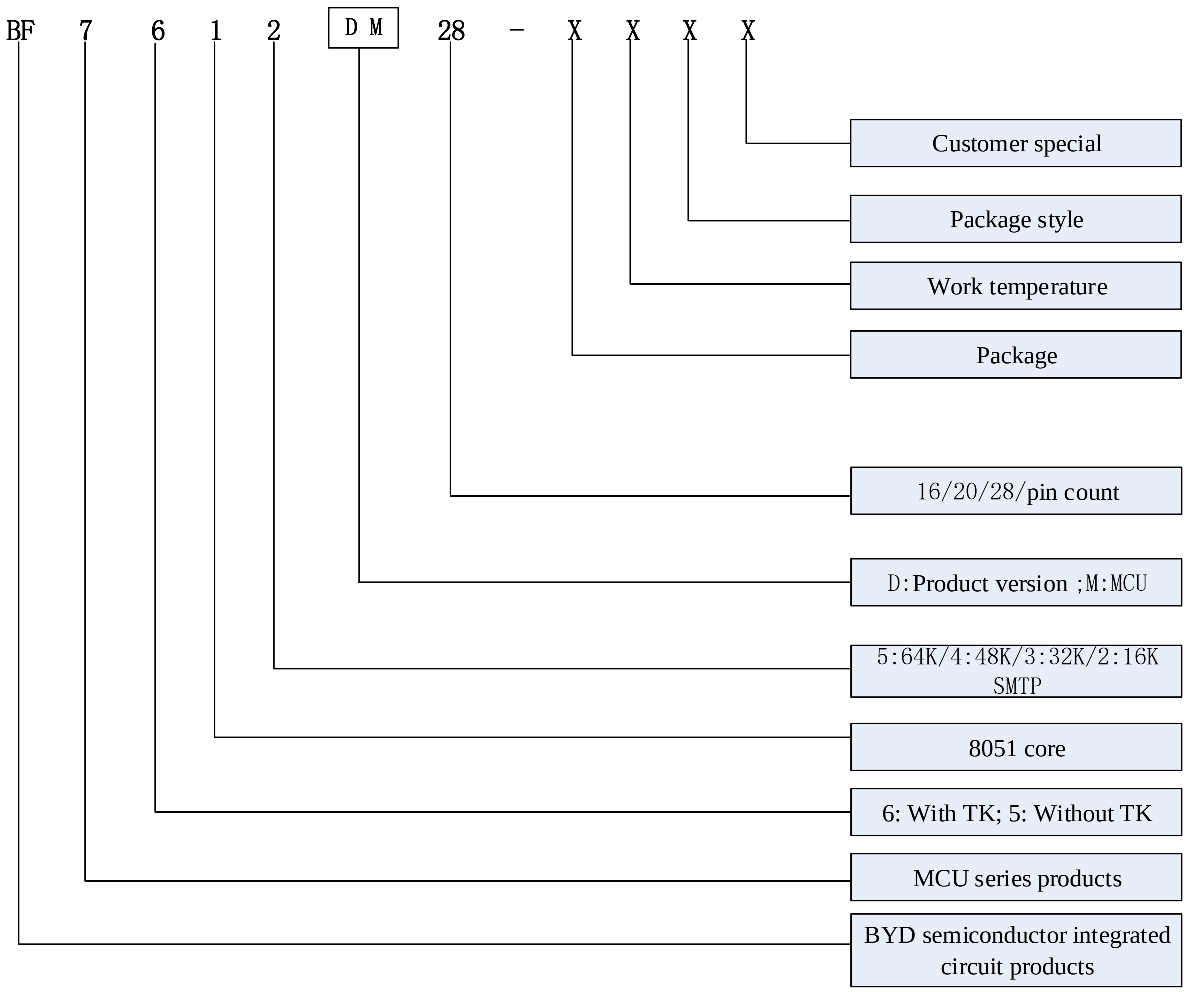
DIM	SOP028 MILLIMETERS		
	MIN	NOM	MAX
A	2.250	2.400	2.650
A1	0.100	0.200	0.300
A2	2.250	2.300	2.350
b	0.300	0.425	0.480
c	0.250	0.285	0.310
D	17.800	18.000	18.200
E1	7.300	7.500	7.700
E	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	-	1
θ	0 °	-	8 °
Face the waste rubber	-	-	0.2
Total length of plastic sealing body	18.000	18.300	18.500

SOP28 package infographic

Ordering Information

Package	Work temperature		Package style	Keep the follow-up
S: SOP	Car grade	A: -40℃~+150℃	B: tap	-
A: SSOP		B: -40℃~+125℃	L: feed tube	-
T: TSSOP		C: -40℃~+105℃	T: tray	-
M: MSSOP		D: -40℃~+85℃	-	-
L: LQFP	Industrial grade	K: -40℃~+85℃	-	-
Q: QFN		J: -40℃~+105℃	-	-
B: BGA		L: -40℃~+125℃	-	-
D: DIP	Consumer grade	P: -25℃~+70℃	-	-
-		Q: 0℃~+70℃	-	-

Example:



Revision Record

Revision date	Revised content	Modifier	Remark
2022-02-18	V1.0	JYY	V1.0
2022-03-02	1. Update BYD LOGO 2. Update input to ADC26_VREF reference voltage voltage selection	YNN	V1.1
2022-03-17	1. Add description of power-on time 2. Update the reference application circuit	YNN	V1.2

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