1. BF7412AMXX-XJLX MCU General Description

1.1. Features

- **Core: 1T 8051**
  - Operating frequency: 6MHz, 3MHz, 2MHz, 1MHz
  - Clock error: ±1% @ -20 ℃ ~65 ℃, 5V
    ±3% @-40 ℃ ~105 ℃, 5V
- **Memory**
  - FLASH: 16K bytes
  - EEPROM: 256 bytes
  - SRAM: 256 bytes(data)+512 bytes(xdata)
- **Clock source, reset**
  - Internal low-speed clock LIRC: 32kHz
    Clock error: ±20% @25 ℃, 5V
    ±35% @-40 ℃ ~105 ℃, 5V
  - Internal high-speed RC oscillator: 1MHz
  - External crystal oscillator: 32768Hz
  - 7 resets, including brown-out reset, brown-out reset 2.8V/3.3V/3.7V/4.2V optional
  - Low voltage detection: 3.0V/3.3V/3.6V/3.9V/4.2V optional
- **IO**
  - PB0~PB7 built-in pull-up/pull-down resistor 28k, other IO built-in pull-up resistor 4.7k
  - High current sink port (PB0~PB7)
  - Support device peripheral function multiplexing
  - All IO ports support external interrupt function, INT0~2 (rising-edge, falling-edge, dual-edge), INT3 shared interrupt source (rising-edge, falling-edge)
- **Communication Module**
  - 2*UART communication, support IO mapping
  - IIC slave mode, support 100/400kHz
- **Operating Voltage: 2.7 V~ 5.5V**
- **Operating Temperature: -40 ℃ ~ 105 ℃**
  - Enhanced industrial grade, in line with JESD industrial grade reliability certification standards
- **16-bit PWM**
  - PWM0 supports multiple groups up to 4 channels, the same frequency, different duty cycle output
  - PWM1/2 support 1 channel output and mapping
- **12-bit High-speed ADC**
  - Up to 26 analog input channels
- **Interrupt**
  - Two-level interrupt priority capablity
  - ADC, CSD, INT0/1/2/3, LVDT, Timer0~2, WDT, UART0/1, IIC interrupt
- **Timer**
  - 2 16-bit Timer0/1, 1 32-bit Timer2
  - Timer2 clock source is internal low-speed clock LIRC 32k or XTAL 32768Hz
  - Watchdog timer, overflow time 18ms to 2.304s
- **Low power mode**
  - Idle mode and sleep mode
  - Deep sleep, power consumption 18μA @5V typical
- **CTK**
  - The key sensitivity is set independently
  - Capacitive keys can be reused as GPIO
- **Two-wire programming, single-wire debugging simulation interface**
- **Package**
  - SOP16/SOP20/SOP28/TSSOP20/TSSOP28

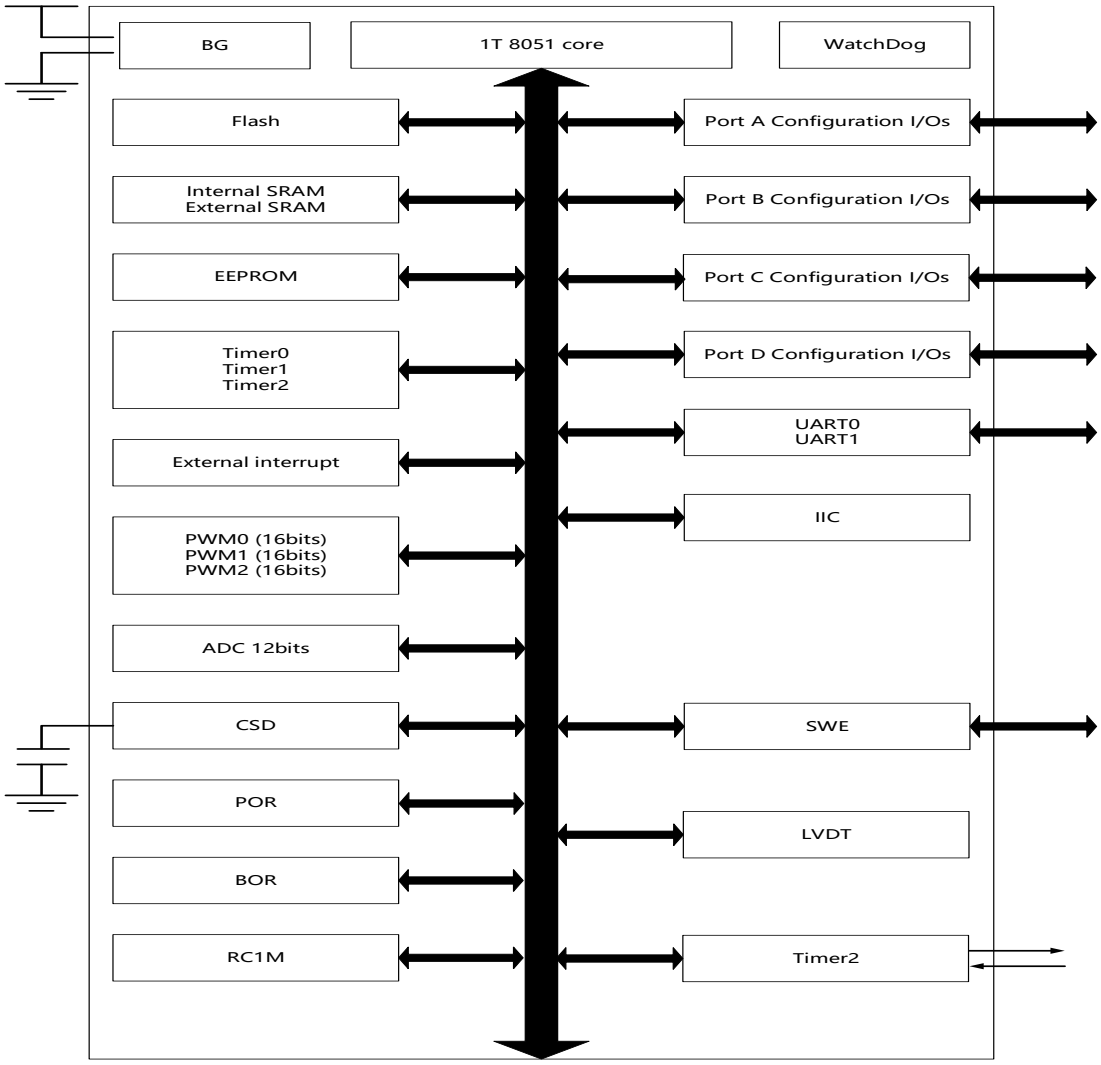
1.2. Overview

The BF7412AMXX-XJLX uses the high speed 8051 core with 1T instruction cycle, compared to the standard 8051 (12T) instruction cycle, has the quicker running speed, compatibility standard 8051 instruction.

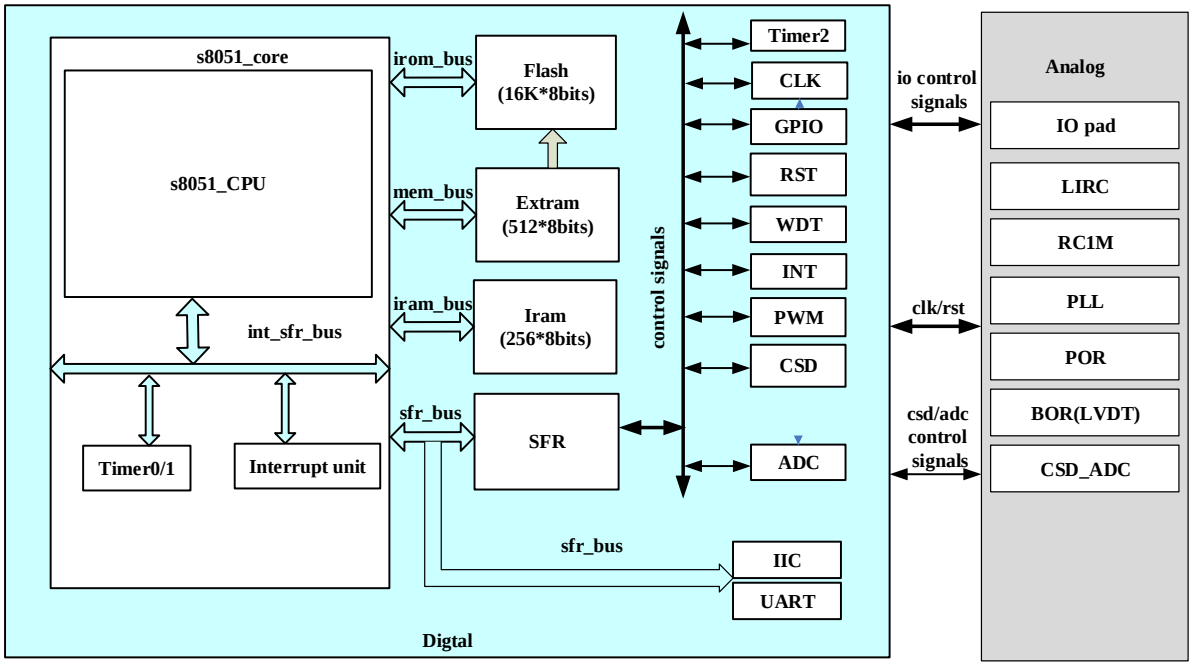
The BF7412AMXX-XJLX includes a watchdog, key detection, IIC, UART, low voltage detection, power down reset, l6-bit PWM, Timer0, Timer1, Timer2, 12-bit successive approximation ADC, low power mode.

The BF7412AMXX-XJLX integrated capacitance channels, which can be used to detect proximity sensing or touch, its built-in MCU, can be flexible configurated, through the configuration can be implemented keys, rollers, sliders and other applications. A key can be run independently, and each key can be adjusted by corresponding special function registers to adjust the sensitivity.

1.3. System Architecture

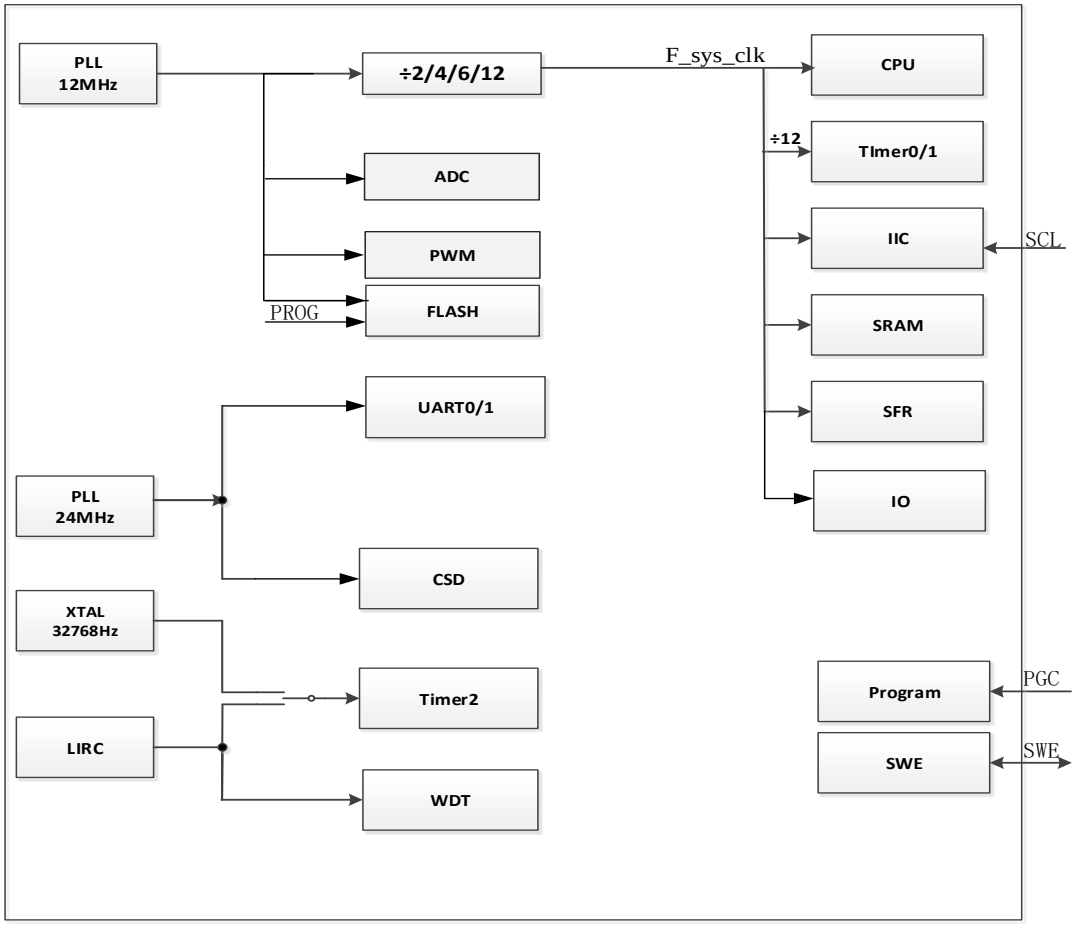


System Architecture



System bus frame diagram

1.4. Clock Diagram



Clock Diagram

1.5. Selection List

Type	BF7412AM16-SJLX	BF7412AM20-SJLX/TJLX	BF7412AM28-SJLX/TJLX
Operating Voltage (V)	2.7~5.5	2.7~5.5	2.7~5.5
Core	1T 8051	1T 8051	1T 8051
Operating Frequency	6M	6M	6M
ROM (Byte)	16K	16K	16K
RAM (Byte)	256+512	256+512	256+512
EEPROM (Byte)	256	256	256
GPIO	14	18	26
KEY	14	18	26
ADC	14	18	26
Timer	3	3	3
PWM	2(4+0+1)	2(4+1+0)	3(4+1+1)
COM	7	8	8
INT	14	18	26
IIC	1	1	1
UART	2	2	2
Package	SOP16	SOP20/TSSOP20	SOP28/TSSOP28

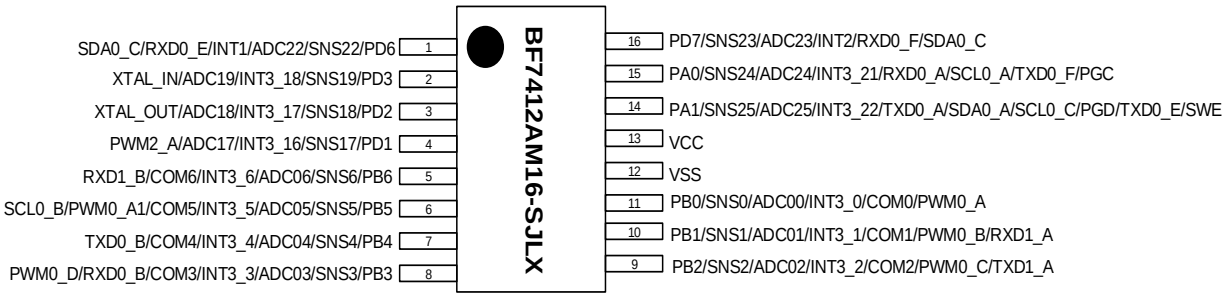
Selection list

Note: PWM module

1. BF7412AM16-SJLX: 2(4+0+1)
   2 represents 2 independent PWM modules, (4+0+1) represents the maximum number of output channels of PWM0+PWM1+PWM2;
2. BF7412AM20-SJLX/TJLX: 2(4+1+0)
   2 represents 3 independent PWM modules, (4+1+0) represents the maximum number of output channels of PWM0+PWM1+PWM2;
3. BF7412AM28-SJLX/TJLX: 3(4+1+1)
   3 represents 3 independent PWM modules, (4+1+1) represents the maximum number of output channels of PWM0+PWM1+PWM2.

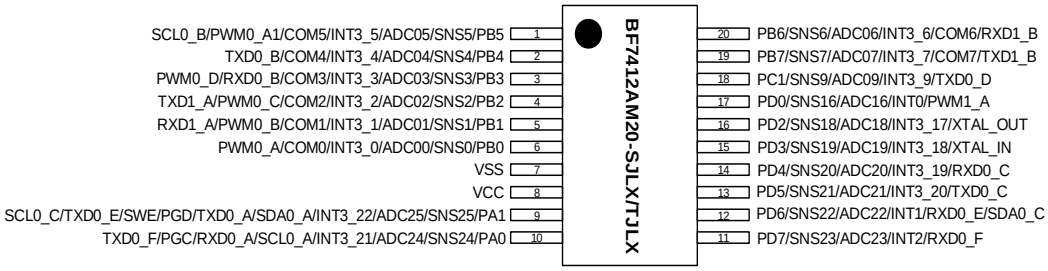
1.6. Pin Assignment

1.6.1. SOP16



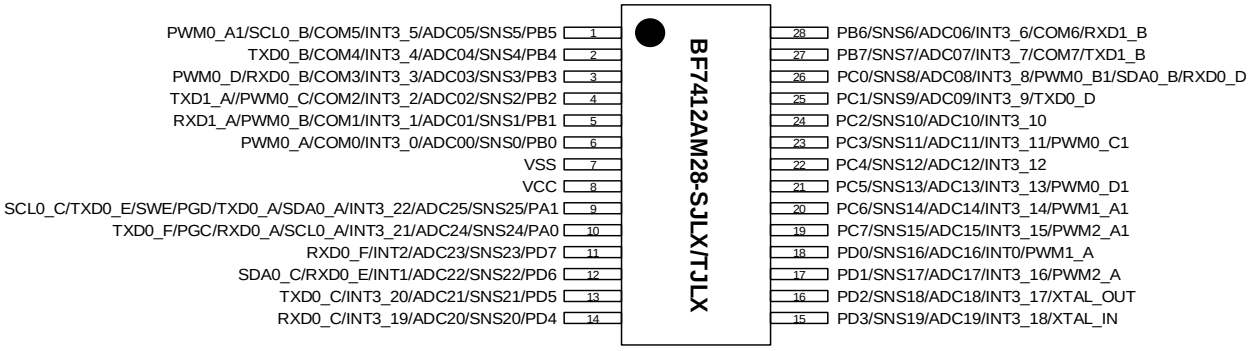
BF7412AM16-SJLX Pin Diagram

1.6.2. SOP20



BF7412AM20-SJLX/TJLX Pin Diagram

1.6.3. SOP28



BF7412AM28-SJTX/TJLX Pin Diagram

1.7. Pin Description

BF7412AM28-SJLX/TJLX	BF7412AM20-SJLX/TJLX	BF7412AM16-SJLX	Function description
1	1		Default function: GPIO <PB5> Other function: SNS5: Touch key channel 5 ADC05: ADC channel 05 INT3_5: External interrupt 3_5 COM5: Large current sink port PWM0_A1: PWM0_A1 output port SCL0_B: Serial clock line of IIC
2	2	7	Default function: GPIO <PB4> Other function: SNS4: Touch key channel 4 ADC04: ADC channel 04 INT3_4: External Interrupt 3_4 COM4: Large current sink TXD0_B: serial pot transmission
3	3	8	Default function: GPIO <PB3> Other function: SNS3: Touch key channel 3 ADC03: ADC channel 03 INT3_3: External Interrupt 3_3 COM3: Large current sink PWM0_D: PWM0_D output port RXD0_B: serial pot reception
4	4	9	Default function: GPIO <PB2> Other function: SNS2: Touch key channel 2 ADC02: ADC channel 02 INT3_2: External interrupt 3_2 COM2: Large current sink port PWM0_C: PWM0_C output port TXD1_A: Serial port transmission
5	5	10	Default function: GPIO <PB1> Other function: SNS1: Touch key channel1 ADC01: ADC channel 01

			INT3_1: External interrupt 3_1 COM1: Large current sink port PWM0_B: PWM0_C output port RXD1_A: serial port receiving
6	6	11	Default function: GPIO <PB0> Other function: SNS0: Touch key channel0 ADC00: ADC channel 00 INT3_0: External interrupt 3_0 COM0: Large current sink port PWM0_A: PWM0_A output port
7	7	12	Default function: GND <VSS>
8	8	13	Default function: Power supply <VCC>
9	9	14	Default function: GPIO <PA1> Other function: SNS25: Touch key channel 25 ADC25: ADC channel 25 INT3_22: External interrupt 3_22 SDA0_A: Serial data line of IIC TXD0_A: Serial port transmission TXD0_E: Serial port transmission SCL0_C: Serial clock line of IIC SWE: Single-wire simulation port PGD: programming port
10	10	15	Default function: GPIO <PA0> Other function: SNS24: Touch key channel 24 ADC24: ADC channel 24 INT3_21: External interrupt 3_21 RXD0_A: serial port receiving TXD0_F: serial port transmission SCL0_A: Serial clock line of IIC PGC: programming port
11	11	16	Default function: GPIO <PD7> Other function: SNS23: Touch key channel 23 ADC23: ADC channel 23 INT2: External interrupt 2 RXD0_F: serial port receiving
12	12	1	Default function: GPIO <PD6> Other function: SNS22: Touch key channel 22 ADC22: ADC channel 22 INT1: External interrupt 1 SDA0_C: Serial data line of IIC RXD0_E: serial port receiving

13	13		Default function: GPIO <PD5> Other function: SNS21: Touch key channel 21 ADC21: ADC channel 21 INT3_20: External interrupt 3_20 TXD0_C: Serial port transmission
14	14		Default function: GPIO <PD4> Other function: SNS20: Touch key channel 20 ADC20: ADC channel 20 INT3_19: External interrupt 3_19 RXD0_C: serial port receiving
15	15	2	Default function: GPIO <PD3> Other function: SNS19: Touch key channel 19 ADC19: ADC channel 19 INT3_18: External interrupt 3_18 XTAL_IN: External crystal oscillator input
16	16	3	Default function: GPIO <PD2> Other function: SNS18: touch key channel 18 ADC18: ADC channel 18 INT3_17: External interrupt 3_17 XTAL_OUT: External crystal oscillator output
17	17	4	Default function: GPIO <PD1> Other function: SNS17: Touch key channel 17 ADC17: ADC channel 17 INT3_16: External interrupt 3_16 PWM2_A: PWM2_A output port
18			Default function: GPIO <PD0> Other function: SNS16: Touch key channel 16 ADC16: ADC channel 16 INT0: External interrupt 0 PWM1_A: PWM1_A output port
19			Default function: GPIO <PC7> Other function: SNS15: Touch key channel 15 ADC15: ADC channel 15 INT3_15: External interrupt 3_15 PWM2_A1: PWM2_A1 output port
20			Default function: GPIO <PC6> Other function: SNS14: Touch key channel 14 ADC14: ADC channel 14 INT3_14: External interrupt 3_14 PWM1_A1: PWM1_A1 output port
21			Default function: GPIO <PC5>

			Other function: SNS13: Touch key channel 13 ADC13: ADC channel 13 INT3_13: External interrupt 3_13 PWM0_D1: PWM0_D1 output port
22			Default function: GPIO <PC4> Other function: SNS12: Touch key channel 12 ADC12: ADC channel 12 INT3_12: External interrupt 3_12
23			Default function: GPIO <PC3> Other function: SNS11: Touch key channel 11 ADC11: ADC channel 11 INT3_11: External interrupt 3_11 PWM0_C1: PWM0_C1 output port
24			Default function: GPIO <PC2> Other function: SNS10: Touch key channel 10 ADC10: ADC channel 10 INT3_10: External interrupt 3_10
25	18		Default function: GPIO <PC1> Other function: SNS9: Touch key channel 9 ADC09: ADC channel 09 INT3_9: External interrupt 3_9 TXD0_D: serial port transmission
26			Default function: GPIO <PC0> Other function: SNS8: Touch key channel 8 ADC08: ADC channel 08 INT3_8: External interrupt 3_8 PWM0_B1: PWM0_B1 output port SDA0_B: Serial data line of IIC RXD0_D: serial port receiving
27	19		Default function: GPIO <PB7> Other function: SNS7: Touch key channel 7 ADC07: ADC channel 07 INT3_7: External interrupt 3_7 COM7: Large current sink port TXD1_B: Serial port transmission
18	20	5	Default function: GPIO <PB6> Other function: SNS6: Touch key channel 6 ADC06: ADC channel 06 INT3_6: External interrupt 3_6 COM6: Large current sink port RXD1_B: serial port receiving

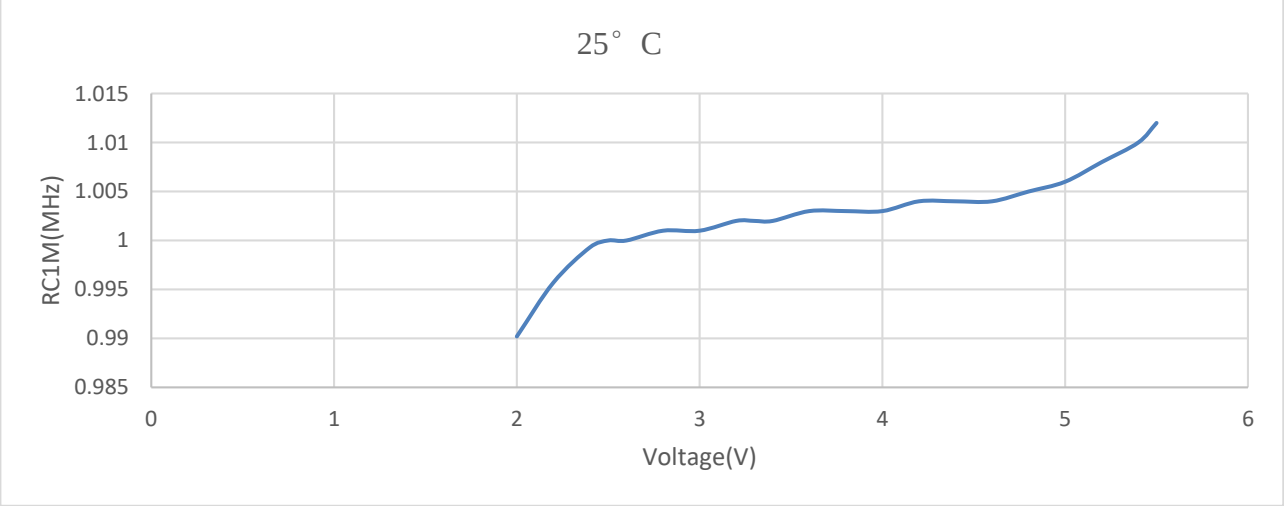
Package pin correspondence diagram

2. Electrical Characteristics

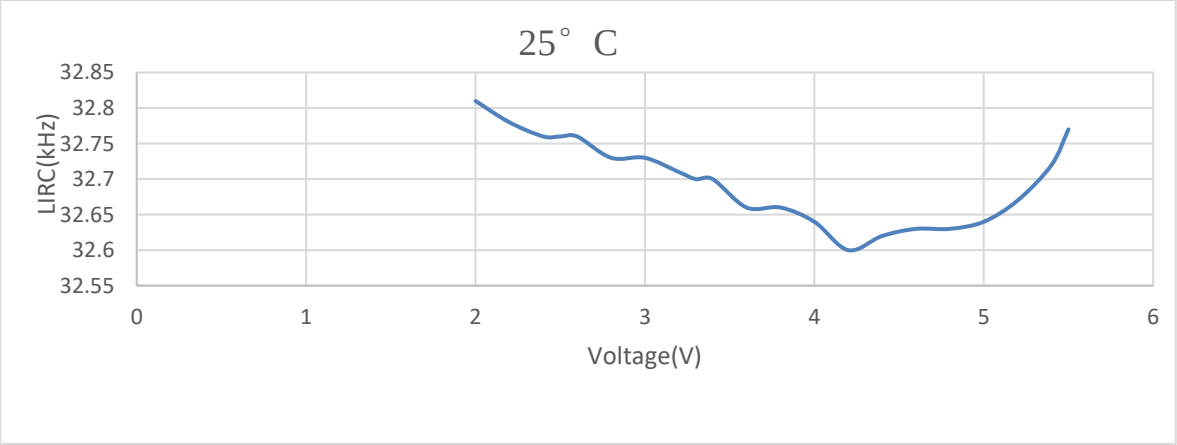
2.1. AC Characteristics

Parameter	Symbol	Condition	Clock skew	Unit
RC	RC1M	Ambient temperature 25 ℃, @5V	±1%	MHz
		Ambient temperature -20 ℃ ~65 ℃, @5V	±1%	
		Ambient temperature -40 ℃ ~105 ℃, @5V	±3%	
		VCC 2.7V~5.5V, ambient temperature 25 ℃	±1%	
System clock	F_sys_clk	Ambient temperature 25 ℃, @5V	±1%	
		Ambient temperature -20 ℃ ~65 ℃, @5V	±1%	
		Ambient temperature -40 ℃ ~105 ℃, @5V	±3%	
		VCC 2.7V~5.5V, ambient temperature 25 ℃	±1%	
WDT clock	LIRC	Ambient temperature 25 ℃, @5V	±20%	kHz
		Ambient temperature -40 ℃ ~105 ℃, @5V	±35%	
		VCC 2.7V~5.5V, ambient temperature 25 ℃	±35%	

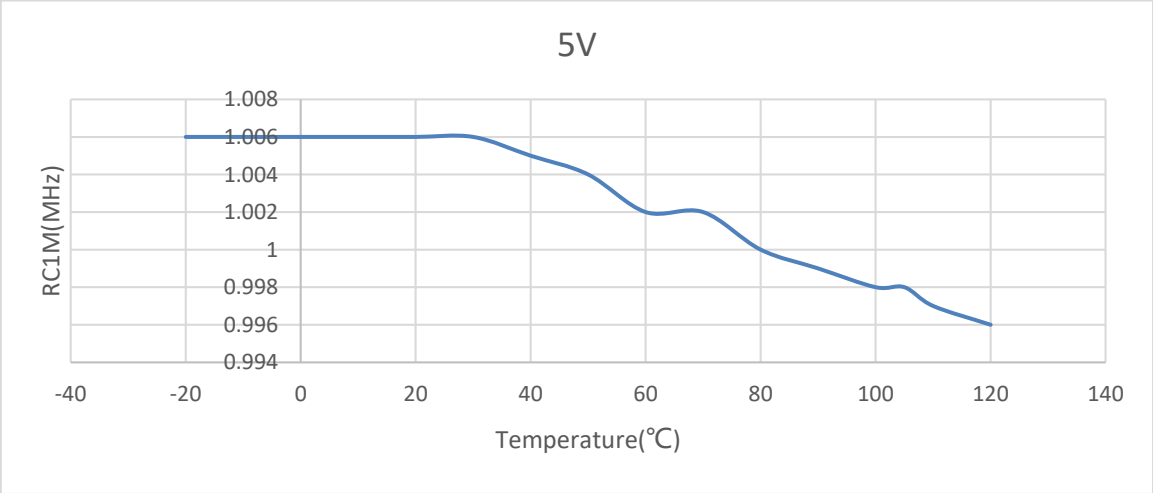
AC characteristics parameters table



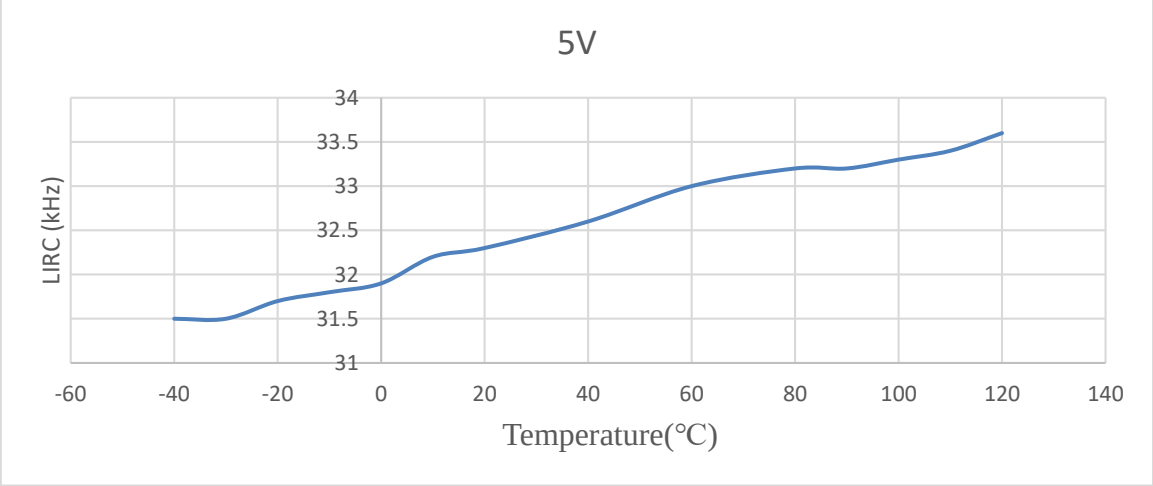
RC1M voltage curve



LIRC voltage curve



RC1M temperature graph



LIRC temperature graph

2.2. DC Characteristics

Unless otherwise stated, typical values are test values at 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	VCC	-	2.7	-	5.5	V
Working mode	Active	@5V, system clock 6M, operating current	-	2.1	2.7	mA
		@5V, system clock 3M, operating current	-	1.3	1.8	mA
		@5V, system clock 2M, operating current	-	1.1	1.5	mA
		@5V, system clock 1M, operating current	-	0.8	1.1	mA
		@3.3V, system clock 6M, operating current	-	1.5	1.9	mA
		@3.3V, system clock 3M, operating current	-	0.9	1.3	mA
		@3.3V, system clock 2M, operating current	-	0.8	1.0	mA
		@3.3V, system clock 1M, operating current	-	0.6	0.8	mA
	Wait	@5V, system clock 6M, IO output low, enter Wait mode, turn off other functions	-	0.5	-	mA
		@3.3V, system clock 6M, IO output low, enter Wait mode, turn off other functions	-	0.4	-	mA
	Idle	@5V, WDT_CTRL=7, WDT interrupt 2s wake up, 2ms working time, IO output low, turn off other functions	-	20	26	μA
		@5V, Timer2 external crystal oscillator 2s wake up, 2ms working time, IO output low, turn off other functions	-	20	26	μA
		@3.3V, WDT_CTRL=7, WDT interrupt 2s wake up, 2ms working time, IO output low, turn off other functions	-	18.5	23	μA
		@3.3V, Timer2 external crystal oscillator 2s wake up, 2ms working time, IO output low, turn off other functions	-	18.5	23	μA
		@5V, CSD parallel mode, WDT interrupt 2s wake up, 2ms working time, IO output low, turn off other functions	-	20	26	μA
		@3.3V, CSD parallel mode, WDT interrupt 2s wake-up, 2ms working time, IO output low, turn off other functions	-	18.5	23	μA
	Sleep	@5V PCON = 0x01, turn off BOR, IO set to low, turn off other functions.	-	18	23	μA
		@3.3V PCON = 0x01, turn off BOR, IO set to low, turn off other functions.	-	17	22	μA
Input low level	V_{IL}	VCC=2.7~5.5V	-	-	0.3*VCC	V

Input high level	V_{IH}	VCC=2.7~5.5V	0.7*VCC	-	-	V
INT Input low level	V_{INTL}	VCC=2.7~5.5V	-	-	0.3*VCC	V
INT Input high level	V_{INTH}	VCC=2.7~5.5V	0.7*VCC	-	-	V
I/O Output Low level	V_{OL}	I_{OL}=4mA@VCC=2.7V, I_{OL}=10mA@VCC=5V	-	-	0.1*VCC	V
I/O Output High level	V_{OH}	I_{OH}=4mA@VCC=2.7V, I_{OH}=10mA@VCC=5V	0.9VCC	-	-	V
IO Sink current	IOL	V_{OL} =0.1VCC, @VCC=5V	-	35	-	mA
IO Source current	IOH	V_{OH} =0.9VCC, @VCC=5V	-	20	-	mA
PB0~PB7 large Sink current	I_{com}	V_{OL} =0.1VCC, @VCC=5V	-	68	-	mA
Input leakage current	I_{Le}	VCC=5V	-	1	5	μA
Pull_up resistor	R_{P_u}	VCC=5V	-	4.7	-	kΩ
Pull_up resistor (PB)	R_{P_u}	VCC=5V	19.6	28	36.4	kΩ
Pull_down resistor (PB)	R_{P_d}	VCC=5V	19.6	28	36.4	kΩ
ADC operating current	I_{ADC}	@5V, system clock 6M, no load, IO output low, enable ADC, open a channel, GET_ADC scan, turn off other functions	-	0.8	-	mA
LVDT operating current	I_{LVDT}	@5V, system clock 6M, no load, low power consumption mode, IO output low, enable LVDT, turn off other functions	-	7.2	-	μA
BOR operating current	I_{BOR}	@5V, system clock 6M, no load, low power consumption mode, IO output low, enable BOR, turn off other functions	-	7.4	-	μA
CSD operating current	I_{CSD}	@5V, system clock 6M, no load, IO output low, open six CSD channels and timer0, turn off other functions	-	0.6	-	mA
PWM operating current	I_{PWM}	@5V, system clock 6M, no load, IO output low , enable PWM0, turn off other functions	-	0.06	-	mA
EEPROM	I_{EEP_E}	@5V, system clock 6M, no load, IO output	-	1.8	-	mA

Erase current		low , enable EEPROM, only erase EEPROM in while, turn off other functions				
EEPROM Write current	I_{EEP_W}	@5V, system clock 6M, no load, low IO output, enable EEPROM, write one byte in while, turn off all other functions	-	1.9	-	mA

DC characteristics parameters table

2.3. ADC Characteristics

Unless otherwise stated, typical values are test values at 25 ℃

ADC electrical characteristics VDD=Vmin-5.5V, GND=0V, TA=+25 ℃						
Parameter	Symbol	Condition	Min	Typical	Max	Unit
Supply voltage	V_{AD}	-	2.7	-	5.5	V
Precision	N_R	-	-	9	10	Bit
A/D input voltage	VAIN	-	VSS	-	V_{REF}	V
A/D input resistance	R_{AIN}	-	-	6.5	17.5	KΩ
A/D working current	I_{AD}	-	-	0.8	-	mA
A/D input current	I_{ADIN}	-	-	-	1	μA
Differential nonlinearity error	DNL	VDD=5.0V	-	±4	±6	LSB
Integral nonlinearity error	INL	VDD=5.0V	-	±4	±6	LSB
ADC sampling time	TAD	-	1.33	-	-	μs
ADC conversion time	TCON	-	7	-	-	μs
Resolution	ADCRESO	-	12			Bit
Input channel	-	-	-	-	30	Channel

ADC characteristics parameters table

2.4. Limit Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage when working	VCC	VSS+2.7	-	VSS+5.5	V
Storage temperature	Tstg	-40	-	125	℃
Operating temperature	Totg	-40	-	105	℃
I/O input voltage	Vin	VSS-0.5	-	VCC+0.5	V
IOL total current	IOLA	-130			mA
IOH total current	IOHA	130			mA
Port electrostatic discharge voltage	ESD(HBM)	-2	-	2	kV

Limit parameters characteristics parameters table

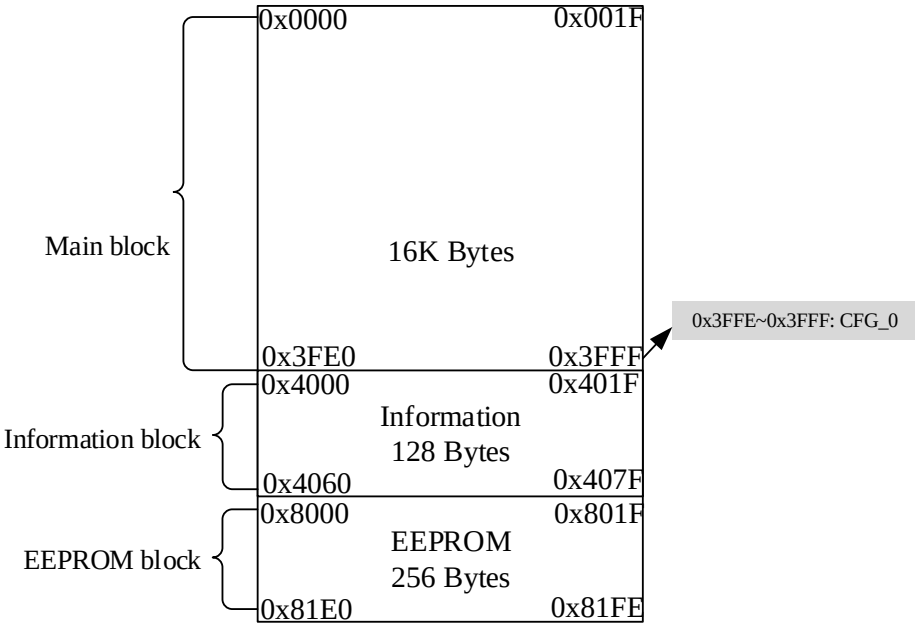
Notes: Exceed the limit parameters may cause damage to the chip, unable to expect the chip work outside the above indicated range. If you work under conditions outside the marked range for a long time, it may affect the reliability of the chip.

3. RAM, FLASH and SFR

3.1. Flash

Features:

- Main block 16KB, can be divided into 8 sectors, each sector 64 pages, 32 Bytes per page
- Information part: 128 Bytes, divided into 4 pages, each page of 32 Bytes
- EEPROM: 256 Bytes, divided into 16 pages, each page of 16 Bytes
- The EEPROM address is 0x8000+2*i (i = 0x00~0xFF)
- In ICP mode, the main block supports block/sector/page erasing, byte writing
- EEPROM supports page erasing and byte writing
- Program/erase times: Program area: at least 10000 times@25℃
  EEPROM: at least 100000 times@25℃
- Data retention: 100 years @25 ℃
  20 years@85℃



Flash Storage Architecture

Main block is mainly used to store the chip program, the address range is 0x0000~0x3FFD, and the configuration word 0 is stored in 0x3FFE~0x3FFF.

The main function of Information block is used to store configuration words, the address range is 0x4000~0x407F.

Steps to read the unique identification code (UID) of the chip:

1. Turn off the interrupt;
2. Read CODE absolute address 0x4072~0x407D corresponding to product ID1~ID12;
3. Restore the interrupt setting.

3.2. RAM

There are 256 Bytes internal, the address is 00H~FFH, including working registers group, bit addressing areas, buffers and SFR, the buffer contain the stack area.

Internal low 128 Bytes, 00H~7FH has 128 Bytes. Read and write data by immediate addressing or indirect addressing.

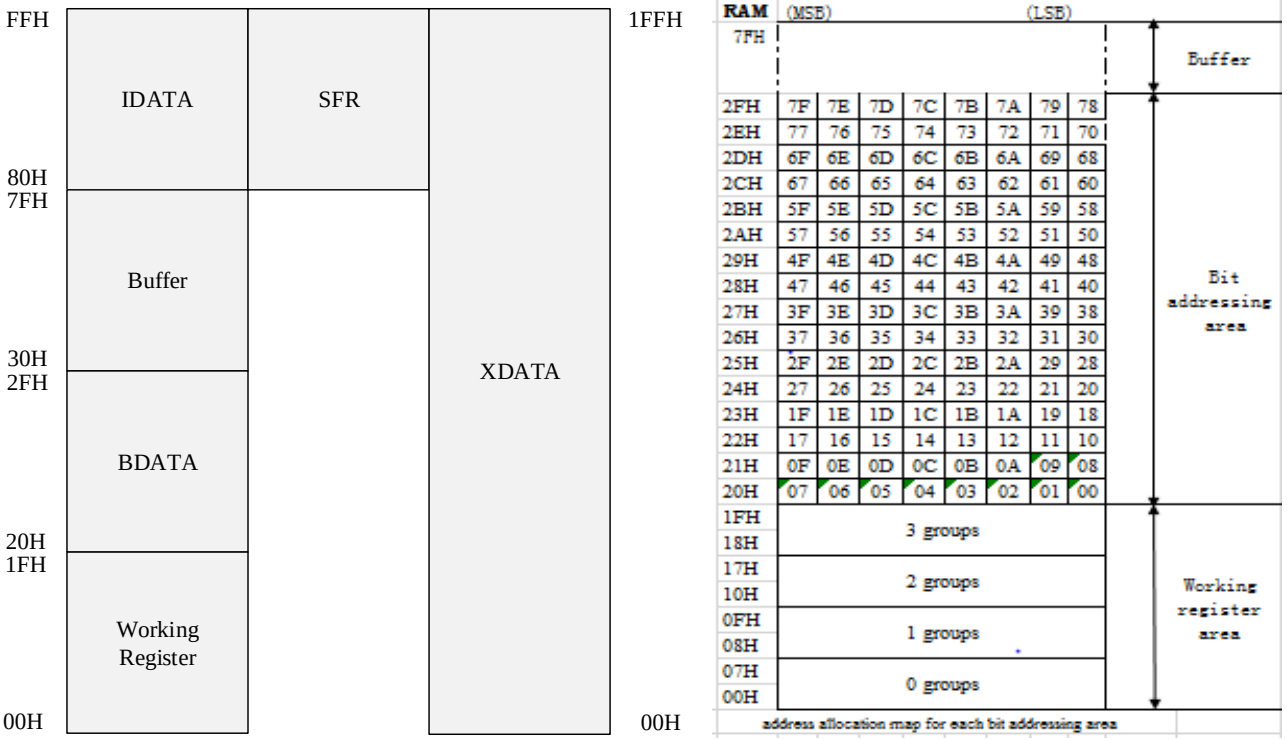
Internal high 128 Bytes, 80H~FFH has 128 Bytes. Read and write data only by immediate addressing or indirect addressing.

Special function register SFR: the address is 80H~FFH, Read and write data only by direct addressing.

Xdata has 512 Bytes, the address is 0000H~01FFH, users can use this area completely. To read and write data through the data pointer or working registers group addressing mode.

Note reserved stack space when writing a program, in order to avoid stack overflow and program goes wrong. Stack first address automatically assigned by program, when programming with C language, but it must be stored in data or idata. KEIL stack can be set in the first address in STARTUP.A51.

RAM address space allocation map:



The following table lists the methods to get value in the three parts of RAM:

DATA	MOV A, direct
	MOV direct, A
	MOV direct, #data
	MOV direct1, direct2
	MOV Rn, direct
	MOV direct, Rn

IDATA	MOV A, @Ri
	MOV @Ri, A
	MOV direct, @Ri
	MOV @Ri, direct
	MOV @Ri, #data

XDATA	MOVX @DPTR, A MOVX A, @DPTR

RAM value instruction set

Notes: n: 0~7, i: 0~1.

3.3. SFR Table

Addr	Name	R/W	Por	Function description
0x80	DATAB	RW	1111_1111b	PB data register
0x81	SP	RW	0000_0111b	Stack pointer register
0x82	DPL	RW	0000_0000b	Data pointer register0 low 8-bit
0x83	DPH	RW	0000_0000b	Data pointer register0 high 8-bit
0x84	SYS_CLK_CFG	RW	xxxx_x001b	Clock control register
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/LVDT buck interrupt status register
0x87	PCON	RW	xxxx_xxx0b	Low-power mode select register
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bits
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bits
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bits
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8 bits
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0x90	DATAC	RW	1111_1111b	PC port data register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow control register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable register
0x93	TIMER2_CFG	RW	xxxx_0000b	TIMER2 CFG register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 count value configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 count value configuration register, low 8 bits
0x98	DATAD	RW	1111_1111b	PD port data register
0x99	PWM1_L_L	RW	0000_0000b	PWM1 low level control register (low 8 bits)
0x9A	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8 bits)
0x9B	PWM1_H_L	RW	0000_0000b	PWM1 high level control register (low 8 bits)
0x9C	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8 bits)
0x9D	PWM2_L_L	RW	0000_0000b	PWM2 low level control register (low 8 bits)
0x9E	PWM2_L_H	RW	0000_0000b	PWM2 low level control register (high 8 bits)
0x9F	PWM2_H_L	RW	0000_0000b	PWM2 high level control register (low 8 bits)
0xA0	P2_XH	RW	1111_1111b	MOVX @Ri,A operation xdata address high 8 bits
0xA1	PWM2_H_H	RW	0000_0000b	PWM2 high level control register (high 8 bits)
0xA2	PWM_EN	RW	xx00_0000b	PWM control register

0xA3	PWM0_CH_CTRL	RW	0000_0000b	PWM0 control register
0xA4	PWM0_CH0_CNT_L	RW	0000_0000b	PWM0 channel 0 count value configuration register low 8 bits
0xA5	PWM0_CH0_CNT_H	RW	0000_0000b	PWM0 channel 0 count value configuration register high 8 bits
0xA6	PWM0_CH1_CNT_L	RW	0000_0000b	PWM0 channel 1 count value configuration register low 8 bits
0xA7	PWM0_CH1_CNT_H	RW	0000_0000b	PWM0 channel 1 count value configuration register high 8 bits
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xA9	PWM0_CH2_CNT_L	RW	0000_0000b	PWM0 channel 2 count value configuration register low 8 bits
0xAA	PWM0_CH2_CNT_H	RW	0000_0000b	PWM0 channel 2 count value configuration register high 8 bits
0xAB	PWM0_CH3_CNT_L	RW	0000_0000b	PWM0 channel 3 count value configuration register low 8 bits
0xAC	PWM0_CH3_CNT_H	RW	0000_0000b	PWM0 channel 3 count value configuration register high 8 bits
0xAD	PWM0_MOD_L	RW	0000_0000b	PWM0 cycle configuration register low 8 bits
0xAE	PWM0_MOD_H	RW	0000_0000b	PWM0 cycle configuration register high 8 bits
0xB1	UART_IO_SEL	RW	xxxx_0000b	UART select enable register
0xB2	PWM_IO_SEL	RW	xx00_0000b	PWM channel selection IO configuration register
0xB3	LVDT_SEL	RW	xx11_1000b	LVDT control register
0xB4	ADC_SPT	RW	0000_0000b	ADC sample time configure register
0xB5	ADC_SCAN_CFG	RW	xx00_0000b	ADC scan control register
0xB6	ADCCKC	RW	xxxx_0000b	ADC clock control register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xB9	ADC_RDATAH	R	xxxx_0000b	ADC scan result register high 4 bits
0xBA	ADC_RDATAL	R	0000_0000b	ADC scan result register low 8 bits
0xBB	ADC_CFG1	RW	0000_0000b	ADC sampling timing control register 1
0xBC	ADC_CFG2	RW	xx00_0111b	ADC sampling timing control register 2
0xBD	UART0_BDL	RW	0000_0000b	UART0 Baudrate control registe
0xBE	UART0_CON1	RW	0000_0000b	UART0 control register 1
0xBF	UART0_CON2	RW	0000_1100b	UART0 control register 2
0xC0	UART0_STATE	RO/RW	x000_0000b	UART0 status flag register
0xC1	UART0_BUF	RW	1111_1111b	UART0 data register
0xC2	PERIPH_IO_SEL3	RW	x000_0000b	INT3 select enable register 3
0xC3	PERIPH_IO_SEL2	RW	0000_0000b	INT3 select enable register 2

0xC4	PERIPH_IO_SEL1	RW	0000_0000b	INT3 select enable register 1
0xC5	UART1_BDL	RW	0000_0000b	UART1 baud rate control register
0xC6	UART1_CON1	RW	0000_0000b	UART1 control register 1
0xC7	UART1_CON2	RW	xxx0_1100b	UART1 control register 2
0xC8	UART1_STATE	RO/RW	x000_0000b	UART1 status flag register
0xC9	UART1_BUF	RW	1111_1111b	UART1 data register
0xCA	CSD_START	RW	xxxx_xxx0b	CSD scan open register
0xCB	SNS_SCAN_CFG1	RW	x000_0000b	Touch key scan configuration register 1
0xCC	SNS_SCAN_CFG2	RW	x100_0000b	Touch key scan configuration register 2
0xCD	SNS_SCAN_CFG3	RW	x111_0000b	Touch key scan configuration register 3
0xCE	CSD_RAWDATAL	R	0000_0000b	CSD counter, low 8-bit
0xCF	CSD_RAWDATAH	R	0000_0000b	CSD counter, high 8-bit
0xD0	PSW	R/RW	0000_0000b	Program status register
0xD1	PULL_I_SELA_L	RW	0000_0000b	CSD pull-up current source selection register
0xD2	SNS_ANA_CFG	RW	xx10_1101b	CSD scan parameter configuration register
0xD3	SNS_IO_SEL1	RW	0000_0000b	SNS channel select register 1
0xD4	SNS_IO_SEL2	RW	0000_0000b	SNS channel select register 2
0xD5	SNS_IO_SEL3	RW	0000_0000b	SNS channel select register 3
0xD6	SNS_IO_SEL4	RW	xxxx_xx00b	SNS channel select register 4
0xD7	RST_STAT	RW	x000_0010b②	Reset flag register
0xD8	PD_PB	RW	0000_0000b	PB port pull-down resistor enable register
0xD9	ADC_IO_SEL1	RW	0000_0000b	ADC function selection register 1
0xDA	ADC_IO_SEL2	RW	0000_0000b	ADC function selection register 2
0xDB	ADC_IO_SEL3	RW	0000_0000b	ADC function selection register 3
0xDC	ADC_IO_SEL4	RW	xxxx_xx00b	ADC function selection register 4
0xDD	PU_PA	RW	xxxx_xx00b	PA port pull-up resistor enable register
0xDE	PU_PB	RW	0000_0000b	PB port pull-up resistor enable register
0xDF	PU_PC	RW	0000_0000b	PC port pull-up resistor enable register
0xE0	ACC	RW	0000_0000b	Accumulator
0xE1	IRCON2	RW	xxxx_x000b	Interrupt flag register 2
0xE2	PU_PD	RW	0000_0000b	PD port pull-up resistor enable register
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit and receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	xxxx_x000b	Interrupt enable register 2
0xE8	IICSTAT	RO/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xEA	TRISA	RW	xxxx_xx11b	PA port direction register

0xEB	TRISB	RW	1111_1111b	PB port direction register
0xEC	TRISC	RW	1111_1111b	PC port direction register
0xED	TRISD	RW	1111_1111b	PD port direction register
0xEE	COM_IO_SEL	RW	0000_0000b	COM port selection configuration register
0xEF	ODRAIN_EN	RW	xxxx_x000b	PA0/PA1/PD6 port open drain enable register
0xF0	B	RW	0000_0000b	B register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF4	IPL2	RW	xxxx_x000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	EXT_INT_CON	RW	x001_0101b	External interrupt polarity control register
0xF8	DATAA	RW	xxxx_xx11b	PA data register
0xFA	SPROG_ADDR_L	RW	0000_0000b	EEPROM address control register
0xFB	SPROG_DATA	RW	xxxx_0000b	EEPROM data register
0xFC	SPROG_CMD	RW	0000_0000b	EEPROM command register
0xFD	SPROG_TIM	RW	xxxx_0001b	EEPROM erase time control register
0xFE	PD_ANA	RW	xxxx_0111b	Module switch control register
0xFF	BOR_SEL	RW	xxx1_1000b①	BOR control register

SFR register summary

Note:

1. **Registers whose addresses end with 8 or 0 can be bit-operated, such as register addresses 0x80, 0x88.**
2. **RO/R: only read. RW: read and write.**
3. **'x' : Indefinite state**
4. **①: The reset value is the default value after the power reset, and the value after the global reset is the factory calibration value.**
5. **②: Power on reset: RST_STAT register reset value 0x02; Other mode reset: The reset flag bit corresponding to the RST_STAT register is 1, and the other reset flag bits remain in the original state.**

3.4. Secondary Bus Register Table

The BF7412AMXX-XJLX series supports expanded secondary bus registers for expanding more register functions. You only need to write the address of the secondary bus register to be accessed into REG_ADDR, and then access the corresponding secondary bus register through the REG_DATA register. It is recommended that when reading and writing secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed. Prevent other interrupts or operations from modifying the address or data of the secondary bus register.

Addr	Name	Bit	R/W	Por	Function description
0x96	REG_ADDR	<5:0>	RW	xx00_0000b	Secondary bus address configuration register
0x97	REG_DATA	<7:0>	RW	0000_0000b	Secondary bus data read and write register

Addr	Name	R/W	Por	Function description
0x00	CFG0_REG	R	1111_1111b①	Configuration word register 0
0x01	CFG1_REG	R	0001_1111b①	Configuration word register 1
0x02	CFG2_REG	R	0011_1111b①	Configuration word register 2
0x03	CFG3_REG	R	1111_1111b①	Configuration word register 3
0x04	CFG4_REG	R	0001_0000b①	Configuration word register 4
0x05	CFG5_REG	RW	1111_1111b①	Configuration word register 5
0x06	CFG6_REG	R	1111_1111b①	Configuration word register 6
0x07	CFG7_REG	R	0000_0011b①	Configuration word register 7
0x08	CFG8_REG	R	1111_1111b①	Configuration word register 8
0x09	CFG9_REG	R	1111_1111b①	Configuration word register 9
0x0A	CFG10_REG	R	1111_1111b①	Configuration word register 10
0x0B	CFG11_REG	R	0000_0011b①	Configuration word register 11
0x0C	CFG12_REG	R	1111_1111b①	Configuration word register 12
0x0D	CFG13_REG	R	1111_1111b①	Configuration word register 13
0x0E	CFG14_REG	R	1111_1111b①	Configuration word register14
0x0F	CFG15_REG	R	0000_0001b①	Configuration word register15
0x10	CFG30_REG	R	1111_1111b①	Configuration word register30
0x1C	OSC_SFR_SEL	RW	xxxx_xx00b	ADJ_OSC selection register

Note:

1.'①': The reset value is the default value after power-on reset, and the value after the global reset is completed is the factory calibration value;

2.'x': Unsteady state;

3.'R': Read only;

4.'RW': Read and write.

4. Register Summary

4.1. SFR Register Detailed Description

DATAB (80H) PB port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	The output level of the PB group can be configured as the GPIO port. The read value is the level state of the current IO port or the configured output value.

SP (81H) Stack pointer register

Bit number	7	6	5	4	3	2	1	0
Symbol	SP[7:0]							
R/W	R/W							
Reset value	7							

DPL(82H) Data pointer register0 low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	DPL[7:0]							
R/W	R/W							
Reset value	0							

DPH (83H) Data pointer register0 high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	DPH[7:0]							
R/W	R/W							
Reset value	0							

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WAIT_MODE	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	WAIT_MODE	WAIT mode enable 1: The chip enters WAIT mode; 0: The chip exits WAIT mode
1~0	PLL_CLK_SEL	PLL clock divided selection register 00: 6MHz; 01: 3MHz; 10: 2MHz; 11: 1MHz

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status, set 0, write WDT_CTRL can set 0. 1: interrupt effective 0: invalid interrupt
0	INT_TIMER2_STAT	TIMER2 interrupt status, set 0, write TIMER2_CFG can set 0. 1: interrupt effective 0: invalid interrupt

INT_POBO_STAT (86H) LVDT boost/LVDT buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	Lvdt boost interrupt status 1: boost interrupt is valid 0: boost interrupt is invaild
0	INT_BO_STAT	Lvdt buck interrupt state 1: buck interrupt is valid 0: buck interrupt is invalid

PCON(87H) Low-power mode select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-		LPM
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	LPM	Low power mode control 1: Low power consumption mode; 0: Normal mode, automatically cleared after waking up Note: After waking up, the software delay must be ≥100μs, otherwise the wake-up function is abnormal

TCON(88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer1 overflow flag. Set to 1 when Timer1 overflows, or Timer0's TH0 overflows in mode three.
6	TR1	Timer1 start enable.When set to 1, enable the Timer1 count or Timer0 TH0 count in mode 3.
5	TF0	Timer0 overflow flag. The hardware set 1 when Timer0 overflows.
4	TR0	Timer0 start enable, when set to 1, start Timer0 count.
3	IE1	External interrupt 1. The hardware set 1, the software is cleared.
1	IE0	External interrupt 0. The hardware set 1, the software is cleared
2, 0	--	Reserved

TMOD(89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer1 mode select bits 00=mode0 – 13-bit timer 01=mode1 – 16-bit timer 10=mode2 – 8-bit auto-reload timers 11=mode3 – Two 8-bit timers

1~0	M0[1:0]	Timer0 mode select bits 00=mode0 – 13-bit timer 01=mode1 – 16-bit timer 10=mode2 – 8-bit auto-reload timers 11=mode3 – Two 8-bit timers

TL0(8AH) Timer 0 counter 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TL1(8BH) Timer 1 counter low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH0(8CH) Timer 0 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

TH1(8DH) Timer 1 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

SOFT_RST(8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Software reset register. Software reset is only generated when the register value is 0x55.

DATAC(90H) PC port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register. The output level of the PC group can be configured as the GPIO port. The read value is the level state of the current IO port or the configured output value.

WDT_CTRL(91H) WDT timing overflow control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~0	WDT_TIME_SEL	WDT overflow timer register. Timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

WDT_EN(92H) WDT timing enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	WDT_EN	WDT timing enable configuration register. WDT is turned off when the configuration value is 0x55.

TIMER2_CFG (93H) TIMER2 CFG register

Bit number	7~4	3	2	1	0
Symbol	-	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
3	TIMER2_CNT_MOD	TIMER2 count step mode select register 1: count step is 65536 clock. 0: count step is 1 clock.
2	TIMER2_CLK_SEL	TIMER2 clock select register 1: select XTAL32768Hz 0: select LIRC
1	TIMER2_RLD	TIMER2 reload enable control register

		1: automatic reload mode 0: manual reload mode
0	TIMER2_EN	TIMER2 count enable register 1: turn on timing; 0: stop timing; In manual reload mode, the hardware automatically clears this register after timing is completed, stop count. In manual reload mode, will maintain the enable register after the count is completed. Automatically re-counting from 0, no matter which mode, configuring this register to 1 during counting will start counting from 0.

TIMER2_SET_H(94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	TIMER2 count configuration register, high 8 bits. Configuring this register during the scan will recount.

TIMER2_SET_L(95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	TIMER2 count configuration register, low 8 bits. Configuring this register during the scan will recount.

DATAD(98H) PD port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD data register. The output level of the PD group can be configured as the GPIO port. The read value is the level state of the current IO port or the configured output value.

PWM1_L_L (99H) PWM1 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_L							
R/W	R/W							
Reset value	0							

PWM1_L_H (9AH) PWM1 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_H							
R/W	R/W							
Reset value	0							

PWM1_H_L (9BH) PWM1 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_L							
R/W	R/W							
Reset value	0							

PWM1_H_H (9CH) PWM1 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H							
R/W	R/W							
Reset value	0							

PWM2_L_L (9DH) PWM2 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_L							
R/W	R/W							
Reset value	0							

PWM2_L_H (9EH) PWM2 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_H							
R/W	R/W							
Reset value	0							

PWM2_H_L (9FH) PWM2 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_L							
R/W	R/W							
Reset value	0							

P2_XH (A0H) MOVX @Ri,A operation xdata address high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	P2_XH	When using the MOVX @Ri, A instruction, when operating the pdata area, P2_XH need to be clear to 0.

PWM2_H_H (A1H) PWM2 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_H							
R/W	R/W							
Reset value	0							

PWM_EN (A2H) PWM control register

Bit number	7	6	5	4
Symbol	-	-	PWM0_CH3_CMOD	PWM0_CH2_CMOD
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH1_CMOD	PWM2_EN	PWM1_EN	PWM0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	PWM0_CH3_CMOD	PWM0 channel 3 duty cycle mode select register 1: select channel 0 duty cycle 0: select its own channel duty cycle
4	PWM0_CH2_CMOD	PWM0 channel 2 duty cycle mode select register 1: select channel 0 duty cycle 0: select its own channel duty cycle
3	PWM0_CH1_CMOD	PWM0 channel 1 duty cycle mode select registe 1: select channel 0 duty cycle 0: select its own channel duty cycle
2~0	PWMn_EN (n=2,1,0)	PWMn module enable register 1: enable; 0: not enable

PWM0_CH_CTRL (A3H) PWM0 control register

Bit number	7	6	5	4
Symbol	PWM0_CH3_ POLA_SEL	PWM0_CH2_ POLA_SEL	PWM0_CH1_ POLA_SEL	PWM0_CH0_ POLA_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH3_EN	PWM0_CH2_EN	PWM0_CH1_EN	PWM0_CH0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	PWM0_CH3_POLA_SEL	Channel 3 polarity selection ch3_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
6	PWM0_CH2_POLA_SEL	Channel 2 polarity selection ch2_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
5	PWM0_CH1_POLA_SEL	Channel 1 polarity selection ch1_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
4	PWM0_CH0_POLA_SEL	Channel 0 polarity selection ch0_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
3	PWM0_CH3_EN	Channel 3 enable ch3_en 1: enable 0: not enable
2	PWM0_CH2_EN	Channel 2 enable ch2_en 1: enable 0: not enable
1	PWM0_CH1_EN	Channel 1 enable ch1_en 1: enable 0: not enable
0	PWM0_CH0_EN	Channel 0 enable ch0_en 1: enable 0: not enable

PWM0_CH0_CNT_L (A4H) PWM0 channel 0 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_L							

R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	PWM0_CH0_CNT_L	Channel 0 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH0_CNT_H (A5H) PWM0 channel 0 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH0_CNT_H	Channel 0 count configuration register high 8 bits. Configure PWM output duty cycle.

PWM0_CH1_CNT_L (A6H) PWM0 channel 1 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH1_CNT_L	Channel 1 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH1_CNT_H (A7H) PWM0 channel 1 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH1_CNT_H	Channel 1 count configuration register high 8 bits. Configure PWM output duty cycle.

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer1 interrupt enable bit 0: Disable timer 1 to apply for interrupt; 1: Allow timer 1 flag bit to apply for interrupt.
2	EX1	INT_EXT1 enable bit 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 interrupt enable bit 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

PWM0_CH2_CNT_L (A9H) PWM0 channel 2 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH2_CNT_L	Channel 2 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH2_CNT_H (AAH) PWM0 channel 2 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH2_CNT_H	Channel 2 count configuration register high 8 bits. Configure PWM output duty cycle.

PWM0_CH3_CNT_L (ABH) PWM0 channel 3 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH3_CNT_L	Channel 3 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH3_CNT_H (ACH) PWM0 channel 3 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH3_CNT_H	Channel 3 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_MOD_L (ADH) PWM0 cycle configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_L	PWM0 count cycle configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_MOD_H (AEH) PWM0 cycle configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_H	PWM0 count cycle configuration register high 8 bits. Configure PWM output duty cycle.

UART_IO_SEL (B1H) UART select enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	UART1_IO_SEL	UART0_IO_SEL		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	UART1_IO_SEL	UART1 port selection enable 0: PB1/2 (RXD1_A/TXD1_A) port select UART1 port function 1: PB6/7 (RXD1_B/TXD1_B) port select UART1 port function
2~0	UART0_IO_SEL	UART0 port selection enable 000: PA0/1 (RXD0_A/TXD0_A) port select UART0 port function 001: PB3/4 (RXD0_B/TXD0_B) port select UART0 port function 010: PD4/5 (RXD0_C/TXD0_C) port select UART0 port function 011: PC0/1 (RXD0_D/TXD0_D) port select UART0 port function 100: PD6/PA1 (RXD0_E/TXD0_E) port select UART0 port function 101: PD7/PA0 (RXD0_F/TXD0_F) port select UART0 port function

PWM_IO_SEL(B2H) PWM channel selection IO configuration register

Bit number	7	6	5	4
Symbol	-	-	PWM2_CH_SEL	PWM1_CH_SEL
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH3_SEL	PWM0_CH2_SEL	PWM0_CH1_SEL	PWM0_CH0_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5	PWM2_CH_SEL	PWM2 channel selection IO port configuration 0: PD1 port selects PWM2 function; 1: PC7 port selects PWM2 function
4	PWM1_CH_SEL	PWM1 channel selection IO port configuration 0: PD0 port selects PWM1 function; 1: PC6 port selects PWM1 function
3	PWM0_CH3_SEL	PWM0 channel 3 select IO port configuration 0: PB3 port selects PWM0_CH3 function;

		1: PC5 port selects PWM0_CH3 function
2	PWM0_CH2_SEL	PWM0 channel 2 selects IO port configuration 0: PB2 port selects PWM0_CH2 function; 1: PC3 port selects PWM0_CH2 function
1	PWM0_CH1_SEL	PWM0 channel 1 select IO port configuration 0: PB1 port selects PWM0_CH1 function; 1: PC0 port selects PWM0_CH1 function
0	PWM0_CH0_SEL	PWM0 channel 0 select IO port configuration 0: PB0 port selects PWM0_CH0 function; 1: PB5 port selects PWM0_CH0 function

LVDT_SEL(B3H) LVDT control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	PD_LVDT	SEL_LVDT_DELAY		SEL_LVDT_VTH		
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	1	1	1	0	0	0

Bit number	Bit symbol	Description
5	PD_LVDT	LVDT control register 1: close; 0: open, close by default
4~3	SEL_LVDT_DELAY	Select signal, select LVDT power-down delay; default 11 0: Delay time 1; 1: Delay time 2; 2: Delay time 3; 3: Delay time 4
2~0	SEL_LVDT_VTH	LVDT threshold selection 000/001: reserved; 010: 3.0V; 011: 3.3V; 100: 3.6V; 101: 3.9V; 11x: 4.2V

ADC_SPT (B4H) ADC sample time configure register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT	ADC sample time configure register sample time: sample_Timer = (ADC_SPT+1)*4Tadc_clk

ADC_SCAN_CFG (B5H) ADC scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	ADC_ADDR					ADC_START
R/W	-	-	R/W					R/W
Reset value	-	-	0					0

Bit number	Bit symbol	Description
5~1	ADC_ADDR	ADC channel address selection register 00000: corresponds to ADC0; 00001: corresponding to ADC1; ... 11001: corresponding to ADC25; 11010: ADC26_VREF; Other values: reserved
0	ADC_START	ADC scan enable register 0: ADC module does not scan; 1: ADC module starts scanning ADC_START is set from 0 to 1, ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit, the ADC interrupt flag bit needs to be cleared by software Note: ADC_START is not allowed to be configured during scanning

ADCCKC (B6H) ADC clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADCCKV		ADCCK	
R/W	-	-	-	-	R/W		R/W	
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3~2	ADCCKV	ADC comparator offset cancellation analog input clock. 0: 12MHz 1: 6MHz 2: 3MHz 3: 2MHz
1~0	ADCCK	ADC_CLK frequency division selection. 0: 3MHz 1: 2MHz 2: 1.5MHz 3: 1MHz

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1(Timer1 interrupt) priority selection bit.

		0: TF1(Timer1 interrupt) is low priority. 1: TF1(Timer1 interrupt) is high priority.
2	PX2	INT_EXT1 interrupt priority selection bit. 0: INT_EXT1 is low priority. 1: INT_EXT1 is high priority.
1	PT0	TF0(Timer0 interrupt) priority selection bit. 0: TF0(Timer0 interrupt) is low priority. 1: TF0(Timer0 interrupt) is high priority.
0	PX0	INT_EXT0 interrupt priority selection bit. 0: INT_EXT0 is low priority. 1: INT_EXT0 is high priority.

ADC_RDATAH (B9H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RAWDATA<11:8>			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	ADC_RAWDATA<11:8>	ADC scan result register

ADC_RDATAL(BAH) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RAWDATA<7:0>							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_RAWDATA<7:0>	ADC scan result register

ADC_CFG1(BBH) ADC sampling timing control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADCWNUM					SAMBG	SAMDEL	
R/W	R/W					R/W	R/W	
Reset value	0					0	0	

Bit number	Bit symbol	Description
7~3	ADCWNUM	Selection of distance conversion interval after sampling 3+ADCWNUM(ADC_CLK)
2	SAMBG	Sampling timing and comparison timing interval selection 0: interval 0; 1: interval 1 (ADC_CLK)
1~0	SAMDEL	Sampling delay time selection 0:0; 1:2; 2:4; 3:8 (ADC_CLK)

ADC_CFG2 (BCH) ADC sampling timing control register 2

Bit number	7	6	5	4
Symbol	-	-	VREF_IN_ADC_SEL	
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	FILTER_R_SEL	ADC_I_SEL		CTRL_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	1	1

Bit number	Bit symbol	Description
5~4	VREF_IN_ADC_SEL	ADC26 internal input voltage selection 00: 1.378V; 01: 2.271V; 10: 3.168V; 11: 4.06V
3	FILTER_R_SEL	Input signal filter selection 0 means no RC filter, 1 means RC filter
2	ADC_I_SEL[1]	ADC bias current size selection register Op amp bias current selection signal 0 is 1uA; 1 is 2uA
1	ADC_I_SEL[0]	ADC bias current size selection register Comparator bias current selection signal 0 is 1uA; 1 is 2uA
0	CTRL_SEL	ADC comparator offset cancellation selection signal 0: First sampling and then offset elimination; 1: All switches are disconnected together

UART0_BDL (BDH) UART0 Baudrate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register. Baud rate modules divisor register lower 8 bits, bandrate={UART0_BDH[1:0], UART0_BDL}, bandrate=0, does not generate baud rate clock. bandrate=1~1023, bandrate = BUSCLK/(16xbandrate)

UART0_CON1 (BEH) UART0 control register 1

Bit number	7	6	5	4
Symbol	UART0_ ENABLE	TRANS_ ENABLE	RECEIVE_ ENABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART0_ENABLE	Module enable. 1: module enable; 0: module off.
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable. 1: receiver open; 0: receiver off.
4	MULTI_MODE	Multiprocessor communication mode. 1: mode enable; 0: mode disable.
3	STOP_MODE	Stop bit width selection. 1: 2 bit; 0: 1 bit.
2	DATA_MODE	Data mode select. 1: 9bit mode; 0: 8bit mode.
1	PARITY_EN	Parity enable. 1: parity enable; 0: parity disable.
0	PARITY_SEL	Parity select. 1: odd parity; 0: even parity.

UART0_CON2 (BFH) UART0 control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	PAD_CHANGE	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	-	R/W	R/W	R/W	R/W	

Reset value	-	-	-	0	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	Txd/rxd pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Send interrupt enable. 1: interrupt enable; 0: interrupt disable (used in polling mode)
2	RX_FULL_IE	Received interrupt enable 1: interrupt enable; 0: interrupt disable (used in polling mode)
1~0	UART0_BDH	Baud rate modulus divisor register high 2bit.

UART0_STATE (C0H) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	Receiver’s ninth data, read only.
5	UART0_T8	Transmitter’s ninth data, read only when parity is enabled.
4	TI0	Send interrupt flag. 1: send buffer is empty; 0: send buffer is full, software write 0 clear 0, write 1 invalid.
3	RI0	Receive interrupt flag. 1: receive buffer is full; 0: receive buffer is empty, software write 0 clear 0, write 1 invalid.
2	UART0_RO	Receive overflow flag; 1: receive overflow (lost new data); 0: no overflow, software write 0 clear 0, write 1 invalid.
1	UART0_F	Framing error flag. 1: framing error flag; 0: no framing error flag, software write 0 clear 0, write 1

		invalid.
0	UART0_P	Parity error flag. 1: receiver parity error; 0: parity is correct, software write 0 clear 0, write 1 invalid.

UART0_BUF (C1H) UART0 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Data register Read returns read-only receive data buffer contents, write into write-only send data buffer.

PERIPH_IO_SEL3(C2H) INT3 select enable register 3

Bit number	7	6	5	4
Symbol	–	INT3_22_IO_SEL	INT3_21_IO_SEL	INT3_20_IO_SEL
R/W	–	R/W	R/W	R/W
Reset value	–	0	0	0
Bit number	3	2	1	0
Symbol	INT3_19_IO_SEL	INT_3_18_IO_SEL	INT3_17_IO_SEL	INT3_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~0	INT3_n_IO_SEL (n=22~16)	INT3_n port selection enable 1: Select INT function; 0: Do not select INT function

PERIPH_IO_SEL2(C3H) INT3 select enable register 2

Bit number	7	6	5	4
Symbol	INT3_15_IO_SEL	INT3_14_IO_SEL	INT3_13_IO_SEL	INT3_12_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_11_IO_SEL	INT3_10_IO_SEL	INT3_9_IO_SEL	INT3_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=15~8)	INT3_n port selection enable 1: Select INT function; 0: Do not select INT function

PERIPH_IO_SEL1(C4H) INT3 select enable register 1

Bit number	7	6	5	4
Symbol	INT3_7_IO_SEL	INT3_6_IO_SEL	INT3_5_IO_SEL	INT3_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_3_IO_SEL	INT3_IO_2_SEL	INT3_1_IO_SEL	INT3_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=7~0)	INT3_n port selection enable 1: Select INT function; 0: Do not select INT function

UART1_BDL(C5H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	-	UART1 baud rate control register The lower 8 bits of the baud rate modulus divisor register, Baud_Mod={UART1_BDH[1:0], UART1_BDL}, When Baud_Mod=0, the baud rate clock is not generated, when Baud_Mod=1~1023, the baud rate = BUSCLK/(16xBaud_Mod)

UART1_CON1 (C6H) UART1 control register 1

Bit number	7	6	5	4
Symbol	UART1_ ENABLE	TRANS_ ENABLE	RECEIVE_E NABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART1_ENABLE	Module enable 1: module enable; 0: module close
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable 1: receiver is on; 0: receiver is off
4	MULTI_MODE	Multiprocessor communication mode 1: mode enable; 0: mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: parity check is enabled; 0: parity check is disabled
0	WAKE_SEL	Parity selection 1: odd parity; 0: even parity

UART1_CON2(C7H) UART1 control register 2

Bit number	7	6	5	4
Symbol	-	-	-	PAD_CHANGE
R/W	-	-	-	R/W
Reset value	-	-	-	0
Bit number	3	2	1	0
Symbol	TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	Txd/rxd pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Transmit interrupt enable 1: interrupt enable; 0: interrupt disabled (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable

		1: interrupt enable; 0: interrupt disabled (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register high 2 bits

UART1_STATE (C8H) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	UART1_R8	UART1_T8	TI1
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART1_R8	The 9th data of the receiver, read only
5	UART1_T8	The 9th data of the transmitter, read only during parity check
4	TI1	Send buffer empty interrupt flag 1: The sending buffer is empty; 0: Send buffer is full, software write 0 to clear
3	RI1	Receive interrupt flag 1: The receive buffer is full; 0: Receive buffer is empty, software write 0 to clear
2	UART1_RO	Receive overflow flag 1: Receive overflow (new data is lost); 0: No overflow, software writes 0 to clear
1	UART1_F	Frame error flag 1: A frame error is detected; 0: No frame error is detected, software writes 0 to clear
0	UART1_P	Parity error flag 1: Receiver parity error; 0: Parity check is correct, software writes 0 to clear

UART1_BUF (C9H) UART1 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	-	Read returns the contents of the read-only receive data

		buffer, writes to the write-only send data buffer.

CSD_START(CAH) CSD scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	-	1: CSD scanning is on; 0: CSD scan stops Write 1 in CSD_START to start scanning. After one scan, the hardware will automatically set to 0. If you want to start the next scan, you need to set it to 1 again by software; if CSD_START=0 during the scan, the scan will stop immediately, and the module will have related internal signals Reset Note: Must be used in accordance with the process configuration: CSD_START=1, if interruption is detected, configure CSD_START=0. CSD_START is not allowed to be configured during scanning

SNS_SCAN_CFG1 (CBH) Touch key scan configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	SW_PRE_OFF	PRS_DIV					
R/W	-	R/W	R/W					
Reset value	-	0	0					

Bit number	Bit symbol	Description
6	SW_PRE_OFF	Front-end charge and discharge clock switch control. 1: close sw_clk; 0: open sw_clk
5~0	PRS_DIV	Front-end charge and discharge clock frequency selection register: 0~61: fixed frequency: F=F24m/2/(PRS_DIV+4) (12M~193K); 62: highest frequency 4M, lowest frequency 1M, center frequency 1.5M, normal distribution; 63: highest frequency 4M, lowest frequency 1M, center frequency 1.5M, normal distribution.

SNS_SCAN_CFG2 (CCH) Touch key scan configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	PULL_I_SELA_H	PARALLEL_EN	CSD_ADDR				
R/W	-	R/W	R/W	R/W				
Reset value	-	1	0	0				

Bit number	Bit symbol	Description
6	PULL_I_SELA_H	CSD pull-up current source configuration highest bit.
5	PARALLEL_EN	SNS channel shunt enable register. 1: multi-channel parallel; 0: signal channel.
4~0	CSD_ADDR	The address of the detection channel 0~25 corresponds to the channel number 0~25

SNS_SCAN_CFG3(CDH) Touch key scan configuration register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-	RESO			CSD_DS		PRE_CHRG_SEL	INIT_DISCHRG_SEL
R/W	-	R/W			R/W		R/W	R/W
Reset value	-	1	1	1	0	0	0	0

Bit number	Bit symbol	Description
6~4	RESO	Counter bit select register. 000: 9 bits; 001: 10 bits; 010: 11 bits; 011: 12bits; 100: 13 bits; 101: 14 bits; 110: 15 bits; 111: 16 bits.
3~2	CSD_DS	Count clock frequency selection register. 00: 24M; 01: 12M; 10: 6M; 11: 4M; default 0.
1	PRE_CHRG_SEL	Pre-charge time selection 0: 20μs; 1: 40μs.
0	INIT_DISCHRG_SEL	Pre-discharge time selection 0: 2μs; 1: 10μs.

CSD_RAWDATAL (CEH) CSD counter, low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	RAWDATA<7:0>							
R/W	R							
Reset value	0							

CSD_RAWDATAH (CFH) CSD counter, high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	RAWDATA<15:8>							
R/W	R							

Reset value	0

PSW(D0H) Program status register

Bit number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS[1:0]		OV	F1	P
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	CY	Carry flag. Set when the addition generates a carry or subtracts a borrow, otherwise clears. Set when the first operand of CJNE is less than the second operand, cleared by MUL or DIV instruction. Also affected by mouse commands (RLC, RRC) and bitwise instructions.
6	AC	Auxiliary carry flag Set when the addition is borrowed from the third to fourth bits of the accumulator, or when the subtraction is borrowed from the third to fourth bits, otherwise cleared.
5	F0	0 flag bit. Universal label for users.
4~3	RS[1:0]	Working register group: Select a valid working register group: RS[1:0] Bank IRAM Area 00 0 0x00-0x07; 01 1 0x08-0x0F; 10 2 0x10-0x17; 11 3 0x18-0x1F
2	OV	Overflow flag bit When the addition produces a different carry of accumulator bits 6 and 7, or subtraction produces a borrow of accumulator bits 6 and 7, otherwise cleared. The OV flag indicates that the signed 8-bit result is out of bounds (greater than 127 or less than -128). The overflow flag is also set when the multiplication result is greater than 255 or an attempt is made to divide by 0.
1	F1	1 flag bit. Universal label for users.
0	P	Parity flag. Always contains the sum of Form 2 of all the bits in the accumulator.

PULL_I_SELA_L (D1H) CSD pull-up current source selection register

Bit number	7	6	5	4	3	2	1	0

Symbol	PULL_I_SEL<7:0>
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	PULL_I_SEL<7:0>	CSD pull up current source size selection switch. The default is 0.

SNS_ANA_CFG (D2H) CSD scan parameter configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	RB_SEL			VTH_SEL		
R/W	-	-	R/W			R/W		
Reset value	-	-	1	0	1	1	0	1

Bit number	Bit symbol	Description
5~4	RB_SEL	Rb resistance size selection. 100: 60k; 101: 80k; Other: reserved Need to read Rb80K calibration value from chip flash when using: CBYTE [0x401E] k/80k, proportional calculation normalization sensitivity.
2~1	VTH_SEL	VTH voltage selection signal 000: 1.4V, 001: 2.1V; 010: 2.5V; 011: 2.8V; 100: 3.2V; 101: 3.5V; 110: 3.9V; 111: 4.1V.

SNS_IO_SEL1(D3H) SNS channel select register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL1 [7:0]	SNS_IO_SEL1 [7:0] corresponds to SNS7~SNS0. The corresponding bit is 1: select SENSOR enable; 0: do not select SENSOR enable

SNS_IO_SEL2 (D4H) SNS channel select register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL2 [7:0]							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL2 [7:0]]	SNS_IO_SEL2[7:0] corresponds to SNS15~SNS8. The corresponding bit is 1: Select SENSOR to enable; 0: Do not select SENSOR enable

SNS_IO_SEL3 (D5H) SNS channel select register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL3 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL3 [7:0]	SNS_IO_SEL3 [7:0] corresponds to SNS23~SNS16. The corresponding bit is 1: Select SENSOR to enable; 0: Do not select SENSOR enable

SNS_IO_SEL4 (D6H) SNS channel select register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	SNS_IO_SEL4[1:0]
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
1~0	SNS_IO_SEL4[1:0]	SNS_IO_SEL4[1:0] corresponds to SNS25~SNS24. The corresponding bit is 1: select SENSOR enable; 0: Do not select SENSOR enable

RST_STAT (D7H) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	--	Reserved
6	DEBUG_F	0: No effect; 1: Trim configuration reset occurred

5	SOFT_F	0: No effect; 1: Software reset occurred
4	PROG_F	0: No effect; 1: A programming reset occurred
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred
2	BO_F	0: No effect; 1: Power-down reset occurred
1	PO_F	0: No effect; 1: Brown-out reset occurred
0	WDTRST_F	0: No effect; 1: Watchdog timer overflow reset occurred

PD_PB(D8H) PB port pull-down resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD_PB7	PD_PB6	PD_PB5	PD_PB4	PD_PB3	PD_PB2	PD_PB1	PD_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PD_PBn (n=7~0)	PB port pull-down resistor enable register 1: The pull-down resistor is enabled; 0: The pull-down resistor is not enabled

ADC_IO_SEL1 (D9H) ADC function selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1[7:0]	ADC_IO_SEL1[7:0] corresponds to ADC07~ADC00. The corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL2(DAH) ADC function selection register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2[7:0]	ADC_IO_SEL2[7:0] corresponds to ADC15~ADC08. The corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL3(DBH) ADC function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3[7:0]	ADC_IO_SEL3[7:0] corresponds to ADC23~ADC16. The corresponding bit is 1: select ADC function; 0: The ADC function is not selected

ADC_IO_SEL4(DCH) ADC function selection register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	ADC_IO_SEL4[1:0]	ADC_IO_SEL4[1:0] corresponds to ADC25~ADC24. The corresponding bit is 1: Select ADC function; 0: Do not select ADC function

PU_PA (DDH) PA port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PU_PA1	PU_PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	--	Port PA pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PB(DEH) PB port pull-up resistor enable register

Bit number		6	5	4	3	2	1	0

Symbol	-
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	--	PB port pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PC(DFH) PC port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PC port pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

ACC(E0H) Accumulator

Bit number	7	6	5	4	3	2	1	0
Symbol	ACC							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ACC	Accumulator The targe register is suitable for all arithmetic and logic operations.

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IE10	IE9	IE8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	IE10	UART1 interrupt flag 1: There is a UART1 interrupt flag; 0: No UART1 interrupt flag

1	IE9	UART0 interrupt flag 1: There is a UART0 interrupt flag; 0: No UART0 interrupt flag
0	IE8	LVDT interrupt flag 1: There is a LVDT interrupt flag; 0: No LVDT interrupt flag

PU_PD (E2H) PD port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PD port pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit receive data buffer

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	–	–	IIC_RST	RD_SCL_EN
R/W	–	–	R/W	R/W
Reset value	–	–	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation 0: IIC module works properly
4	RD_SCL_EN	Host read pull low clock line control bit. 1: enable the host to read and pull the low clock line function; 0: disable the host to read and pull the low clock line function.
3	WR_SCL_EN	Host write pull low clock line control bit. 1: enable the host to write and pull the low clock line function; 0: disable the host to write and pull the low clock line function.
2	SCLEN	IIC clock enable bit 1: clock work properly 0: pull down the clock line.
1	SR	IIC conversion rate control bit 1: conversion rate control is turned off to adapt to the standard speed mode (100K); 0: conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC normal work; 0: IIC not work

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable
6	EX6	External interrupt 3 interrupt enable 1: Interrupt enable; 0: Interrupt disable
5	EX5	CSD interrupt enable 1: interrupt enable; 0: interrupt disable
4	EX4	ADC interrupt enable 1: interrupt enable; 0: interrupt disable
3	EX3	IIC interrupt enable 1: interrupt enable; 0: interrupt disable
2	EX2	External interrupt 2 interrupt enable

		1: interrupt enable; 0: interrupt disable
1~0	-	Reserved

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	EX10	EX9	EX8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~3	-	Reserved
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable
0	EX8	LVDT interrupt enable 1: interrupt enable; 0: interrupt disable

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: boot bit detected; 0: no boot bit detected
6	IIC_STOP	Stop signal flag 1: stop status detected; 0: no stop status detected
5	IIC_RW	Read and write flag. Record the read/write information obtained from the address byte after the last address match. 1: read; 0: write.

4	IIC_AD	Address data flag bit. 1: indicates that the most recently received or sent byte is data; 0: indicates that the most recently received or sent byte is address.
3	IIC_BF	IICBUF full flag. Received in IIC bus mode: 1: received successfully, buffer is full; 0: received successfully, buffer is empty. Send in IIC bus mode: 1: data transmission is in progress (does not include the acknowledge bit and the stop bit), buffer is full; 0: data transmission has been completed (does not include the acknowledge bit and the stop bit), buffer is empty.
2	IIC_ACK	Answer flag 1: invalid response signal; 0: effective response signal.
1	IIC_WCOL	Write conflict flag. 1: when the IIC is transmitting the current data, the new data is attempted to be written to the transmit buffer; new data cannot be written to the buffer. 0: no write conflict
0	IIC_RECOV	Receive overflow flag bit 1: When the previous data received by the IIC has not been taken, new data is received, the new data cannot be received by the buffer. 0: no receive overflow.

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

TRISA (EAH) PA port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA direction register, 0: output; 1: input

TRISB(EBH) PB port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB direction register, 0: output; 1: input

TRISC(ECH) PC port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC direction register, 0: output; 1: input

TRISD(EDH) PD port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD direction register, 0: output; 1: input

COM_IO_SEL (EEH) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, PB port corresponds to bit selection 1: Select the COM port mode and turn on the high current function; 0: select IO port mode

ODRAIN_EN (EFH) PA0/PA1/PD6 port open drain enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	--	PA0/PA1/PD6 open-drain output enable register Bit[0]: PA0, Bit[1]: PA1, Bit[2]: PD6 1: Open drain output; 0: CMOS output

B (F0H) B register

Bit number	7	6	5	4	3	2	1	0
Symbol	B							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	B	B register: the source and destination registers of multiplication and division operations.

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: There is a WDT/Timer2 interrupt flag; 0: No WDT/Timer2 interrupt flag
6	IE6	External interrupt 3 interrupt flag 1: There is a External interrupt 3interrupt flag; 0: No External interrupt 3 interrupt flag
5	IE5	CSD interrupt flag 1: There is a CSD interrupt flag; 0: No CSD interrupt flag
4	IE4	ADC interrupt flag 1: There is a ADC interrupt flag; 0: No ADC interrupt flag
3	IE3	IIC interrupt flag

		1: There is a IIC interrupt flag; 0: No IIC interrupt flag
2	IE2	External interrupt 2 interrupt flag 1: There is a INT2 interrupt flag; 0: No INT2 interrupt flag
1~0	–	Reserved

PERIPH_IO_SEL (F2H) IIC /INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	IIC_IO_SEL	
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	1	0	0	0
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
6	IIC_AFIL_SEL	IIC port analog filter selection enable 1: select analog filter function; 0: do not select analog filter function.
5	IIC_DFIL_SEL	IIC port digital filter selection enable. 1: select digital filter function; 0: do not select digital filter function.
4~3	IIC_IO_SEL	IIC select enable 0: PA0/PA1 select IIC function; 1: PB5/PC0 select IIC function; 2: PA1/PD6 select IIC function (When PB5/PC0 is used as IIC port, there is no SR control function, automatic logic control becomes open-drain output, when PB5/PC0 is used as GPIO, there is no open-drain output function)
2	INT2_IO_SEL	INT2 select enable, correspond PD7 1: select INT2 function 0: not select INT2 function
1	INT1_IO_SEL	INT1 select enable, correspond PD6 1: select INT1 function 0: not select INT1 function
0	INT0_IO_SEL	INT0 select enable, correspond PD0 1: select INT0 function 0: not select INT0 function

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	IPL2.2	UART1 interrupt priority. 0: low priority; 1: high priority
1	IPL2.1	UART0 interrupt priority. 0: low priority; 1: high priority
0	IPL2.0	LVDT interrupt priority. 0: low priority; 1: high priority

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority
6	IPL1.6	External interrupt 3 interrupt priority. 0: low priority; 1: high priority
5	IPL1.5	CSD interrupt priority. 0: low priority; 1: high priority
4	IPL1.4	ADC interrupt priority. 0: low priority; 1: high priority
3	IPL1.3	IIC interrupt priority. 0: low priority; 1: high priority
2	IPL1.2	External interrupt 2 priority. 0: low priority; 1: high priority
1~0	--	Reserved

EXT_INT_CON (F7H) External interrupt polarity control register

Bit number	7	6	5	4
Symbol	-	INT3_POLARITY	INT2_POLARITY	
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1

Bit number	3	2	1	0
Symbol	INT1_POLARITY		INT0_POLARITY	
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1

Bit number	Bit symbol	Description
6	INT3_POLARITY	External interrupt 3_x trigger polarity selection: 1: Rising edge (high level wake-up in low power mode) 0: Falling edge (low-level wake-up in low-power mode)
5~4	INT2_POLARITY	External interrupt 2 trigger polarity selection: 01: Falling edge (low-level wake-up in low-power mode) 10: rising edge (high level wake-up in low power mode) 00/11: Double edge (low-level wake-up in low-power mode)
3~2	INT1_POLARITY	External interrupt 1 trigger polarity selection: 01: Falling edge (low-level wake-up in low-power mode) 10: rising edge (high level wake-up in low power mode) 00/11: Double edge (low-level wake-up in low-power mode)
1~0	INT0_POLARITY	External interrupt 0 trigger polarity selection: 01: Falling edge (low-level wake-up in low-power mode) 10: rising edge (high level wake-up in low power mode) 00/11: Double edge (low-level wake-up in low-power mode)

DATAA (F8H) PA data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PA1	PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA data register. The output level of the PA group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

SPROG_ADDR_L(FAH) EEPROM address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description

7~0	--	EEPROM block address low 8 bits SPROG_ADDR_L [3:0]: select the address in the page, SPROG_ADDR_L [7:4]: select the page.

SPROG_DATA(FBH) EEPROM data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	EEPROM programming: the number of data to be written (0~15) (SPROG_NUM*2bytes) When SPROG_NUM=0, it means that only 1 data is programmed

SPROG_CMD(FCH) EEPROM command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: EEPROM page erase; Write 0x69: EEPROM byte programming

SPROG_TIM (FDH) EEPROM erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset value	–	–	–	–	0	0	1	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3~2	--	0~3 data writing time=1.50~2.25ms (step 0.25ms) 00: Data writing time=1.50ms; 01: Data writing time = 1.75ms; 10: Data writing time=2.00ms; 11: Data writing time = 2.25ms Note: The time for writing single or multiple words is the time selected above
1~0	--	0~3 page erasing time=2.25~3.00ms (step 0.25ms)

		00: page erasing time = 2.25ms; 01: Page erasing time=2.50ms; 10: Page erase time=2.75ms; 11: Page erase time=3.00ms

PD_ANA (FEH) Module switch control register

Bit number	7~4	3	2	1	0
Symbol	-	PD_OSC_32K	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	1	1	1

Bit number	Bit symbol	Description
3	PD_OSC_32K	LIRC control register 1: off; 0: on, default on
2	PD_XTAL_32K	RTC crystal oscillator circuit (32768Hz) control register. 1: close; 0: open; default close.
1	PD_CSD	Analog CSD work control register: 0: CSD module works normally; 1: CSD module does not work
0	PD_ADC	Analog ADC shutdown control register 0: ADC module works normally; 1: ADC module does not work

BOR_SEL(FFH) BOR control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	PD_BOR	SEL_BOR_DELAY	SEL_BOR_VTH		
R/W	-	-	-	R/W	R/W	R/W		
Reset value	-	-	-	1	1	0		

Bit number	Bit symbol	Description
4	PD_BOR	BOR control register 1: close; 0: open, close by default Note: It is recommended to open BOR without delay when the program is first initialized
3	SEL_BOR_DELAY	Select the signal, select the power-down delay of BOR 0: Delay time 1; 1: Delay time 2
2~0	SEL_BOR_VTH	BOR threshold selection 000: reserved; 001: 2.8V; 010: 3.3V; 011: 3.7V; 1xx: 4.2V

Note:

1. The reserved register and the reserved bits of the register are forbidden to write operation, otherwise the chip may be abnormal.

4.2. Secondary Bus Registers Detailed Description

CFG0_REG (00H) Configuration word register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG0_REG[7:0]							
R/W	R							
Reset value	FF							

CFG1_REG (01H) Configuration word register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG1_REG[7:0]							
R/W	R							
Reset value	1F							

CFG2_REG (02H) Configuration word register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG2_REG[7:0]							
R/W	R							
Reset value	3F							

CFG3_REG (03H) Configuration word register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG3_REG[7:0]							
R/W	R							
Reset value	FF							

CFG4_REG (04H) Configuration word register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG4_REG[7:0]							
R/W	R							
Reset value	10							

CFG5_REG (05H) Configuration word register 5

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG5_REG[7:0]							
R/W	R							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	-	Configuration word register The written value is SFR, the read value is the effective value,

		and the configuration word or SFR is selected according to OSC_SFR_SEL

CFG6_REG (06H) Configuration word register 6

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG6_REG[7:0]							
R/W	R							
Reset value	FF							

CFG7_REG (07H) Configuration word register 7

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG7_REG[7:0]							
R/W	R							
Reset value	03							

CFG8_REG (08H) Configuration word register 8

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG8_REG[7:0]							
R/W	R							
Reset value	FF							

CFG9_REG (09H) Configuration word register 9

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG9_REG[7:0]							
R/W	R							
Reset value	FF							

CFG10_REG (0AH) Configuration word register 10

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG10_REG[7:0]							
R/W	R							
Reset value	FF							

CFG11_REG (0BH) Configuration word register 11

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG11_REG[7:0]							
R/W	R							
Reset value	03							

CFG12_REG (0CH) Configuration word register 12

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG12_REG[7:0]							
R/W	R							
Reset value	FF							

CFG13_REG (0DH) Configuration word register 13

Bit number	7	6	5	4	3	2	1	0

Symbol	CFG13_REG[7:0]
R/W	R
Reset value	FF

CFG14_REG (0EH) Configuration word register 14

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG14_REG[7:0]							
R/W	R							
Reset value	FF							

CFG15_REG (0FH) Configuration word register 15

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG15_REG[7:0]							
R/W	R							
Reset value	01							

CFG30_REG (10H) Configuration word register 16

Bit number	7	6	5	4	3	2	1	0
Symbol	CFG30_REG[7:0]							
R/W	R							
Reset value	FF							

OSC_SFR_SEL(1CH) ADJ_OSC selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	--	Register ADJ_OSC effective value selection 10: Select SFR write value; Other: select configuration word Note: Read the OSC calibration value and control it within ±10% of the CFG5_REG[7:0] calibration value

REG_ADDR (96H) Secondary bus address configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	REG_ADDR[5:0]					
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	0	0	0	0	0	0

Bit number	Bit symbol	Description
5~0	REG_ADDR[5:0]	Secondary bus address configuration register When operating the secondary bus register, it is

		recommended to read and write the secondary bus register, first EA = 0, and then EA = 1 after the operation is completed, to prevent other interrupts or operations from modifying the address or data of the secondary bus register

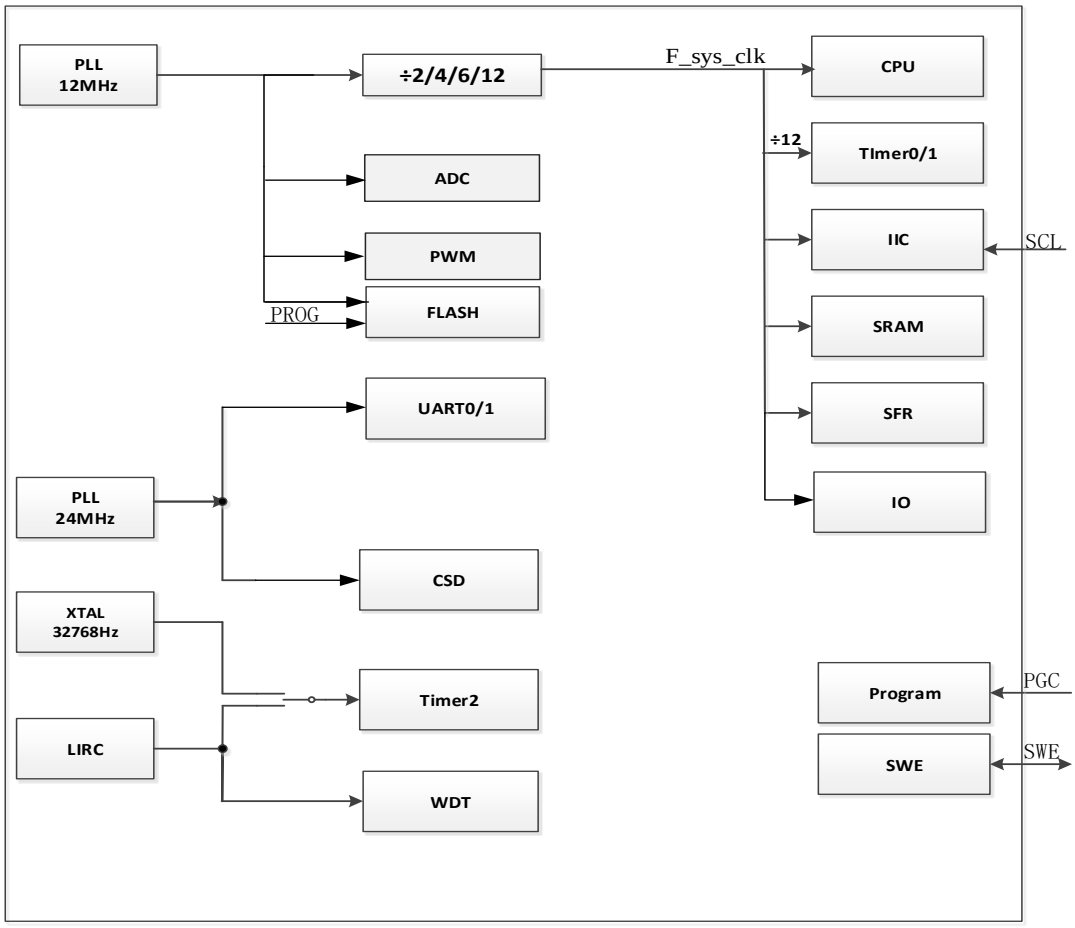
REG_DATA (97H) Secondary bus data read and write registers

Bit number	7	6	5	4	3	2	1	0
Symbol	REG_DATA[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	REG_DATA[7:0]	Secondary bus data read and write registers: It is recommended to read and write secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed, to prevent other interrupts or operations from modifying the secondary bus register address or data

5. Clock, Reset, Work Mode, WDT

5.1. Clock Definition



Clock block diagram

The BF7412AMXX-XJLX series clock is defined as follows:

PLL_12MHz: Frequency 12MHz, gate control module enabled, used as ADC, Flash, PWM control, clock source and system clock after frequency division.

F_sys_clk: Frequency 6MHz/3MHz/2MHz/1MHz, which can be used as a core-related clock.

XTAL32768Hz: external 32768 Hz precision clock, which can be used as Timer2 clock.

RC1MHz: built-in RC oscillator with a frequency of 1MHz and PLL clock.

LIRC: internal low-speed clock, this clock is used as watchdog clock and Timer2 clock.

PLL_24MHz: The frequency is 24MHz, the gating module is enabled, and it is used as the CSD and UART clock source.

SCL: IIC master clock, sent by the IIC Master, as the IIC communication clock.

PGC: Programming clock, download clock when programming and burning programs.

5.2. Clock Related Registers

SYS_CLK_CFG (84H) Clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WAIT_MODE	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	WAIT_MODE	WAIT mode enable 1: The chip enters WAIT mode; 0: The chip exits WAIT mode
1~0	PLL_CLK_SEL	PLL clock divided selection register 00: 6MHz; 01: 3MHz; 10: 2MHz; 11: 1MHz

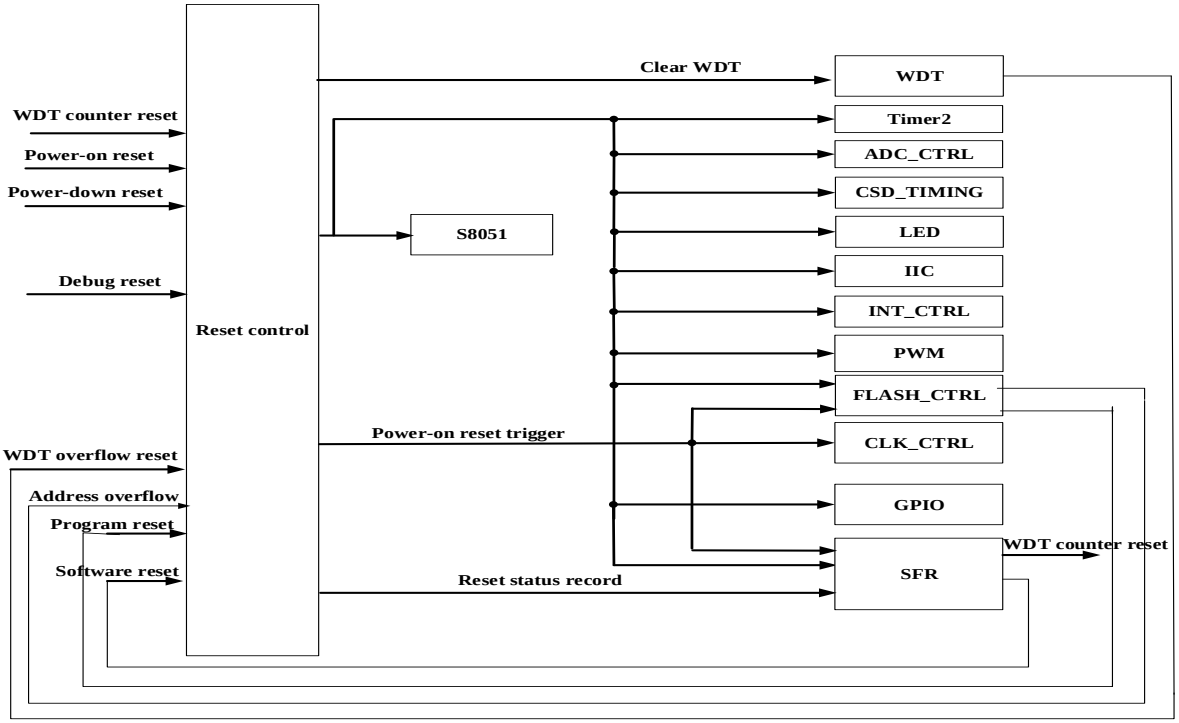
PD_ANA (FEH) Module switch control register

Bit number	7~4	3	2	1	0
Symbol	-	PD_OSC_32K	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	1	1	1

Bit number	Bit symbol	Description
3	PD_OSC_32K	LIRC control register 1: off; 0: on, default on
2	PD_XTAL_32K	RTC crystal oscillator circuit (32768Hz) control register. 1: close; 0: open; default close.

5.3. Reset

There are 7 reset modes in BF7412AMXX-XJLX: WDT overflow reset (WDTRST_F), power on reset (PO_F), brown-out reset (BO_F), program reset (PROG_F), debug reset (DEBUG_F), PC pointer overflow reset (ADDROF_F), software reset (SOFT_F). Any one of above reset, global will make chip reset. We can judge the reset flag register which reset happen, the reset must be cleared by software.



Reset block diagram

5.3.1. Reset sequence

po_n: Power-on reset, the analog module is generated after the system is powered on, and the system exits the reset mode.

bo_n: Power-down reset, the analog module generates a low-level signal after the system has a power-down reset. When the power-down reset signal is low, the entire chip is in the reset state. After the global reset signal becomes high, the system exits the reset mode after the global reset signal continues to be valid for 20ms.

prog_en: Programming reset. When prog_en is high, it is the programming mode of FLASH. At this time, the global reset signal is valid. After it goes low, the global reset signal continues to be valid for 20ms.

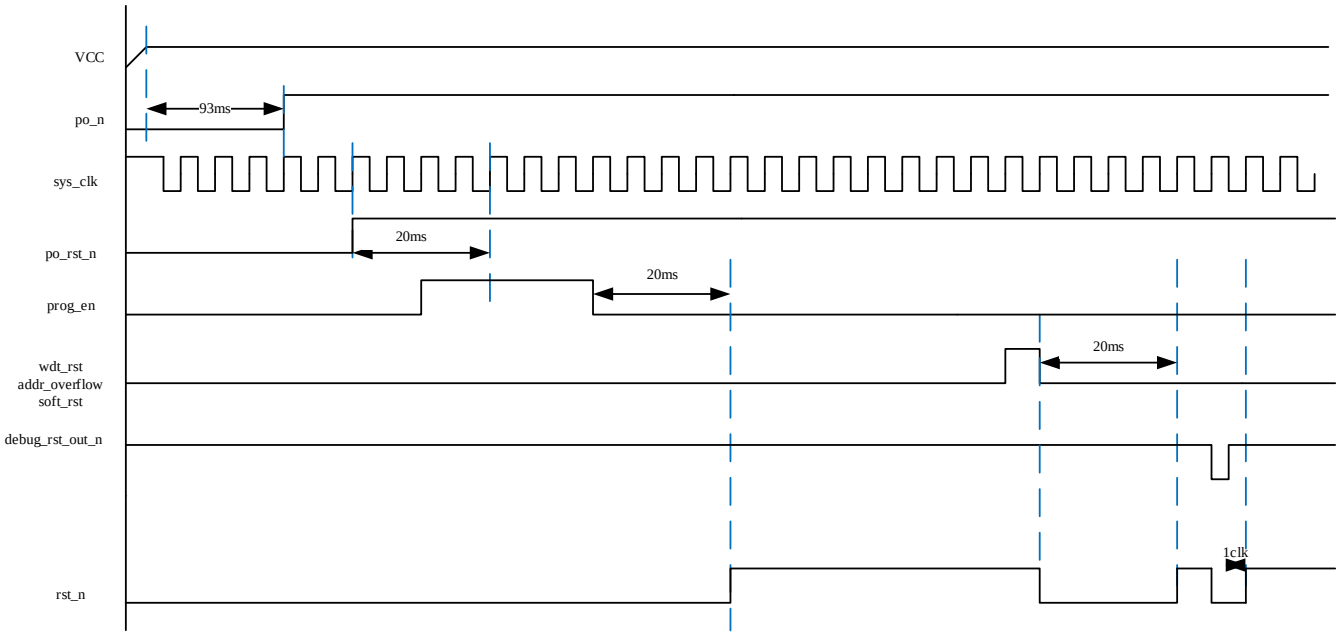
soft_rst: software reset, the soft reset signal is valid by writing SFR, and the global reset signal is valid for 20ms. After 20ms, the system exits the reset mode.

wdt_rst: The watchdog timer overflows and resets. After the watchdog timer overflows, the global

reset is 20ms. After 20ms, the system exits the reset mode.

addr_overflow: PC pointer overflow reset. If the PC pointer exceeds the valid address range of the flash when the MCU addresses the program memory, the addr_overflow signal becomes high, and the sys_clk clock rising edge detects the high level of addr_overflow (requires 1 clock cycle) and resets the global 20ms, the reset signal will clear the addr_overflow signal to zero. After 20ms, the system exits the reset mode.

debug_rst_out_n: trim configuration reset, output a reset signal for the core trim module, low means reset is effective, chip global reset, but there will not be a 20ms initialization process, only delay 1 system clock reset low level.

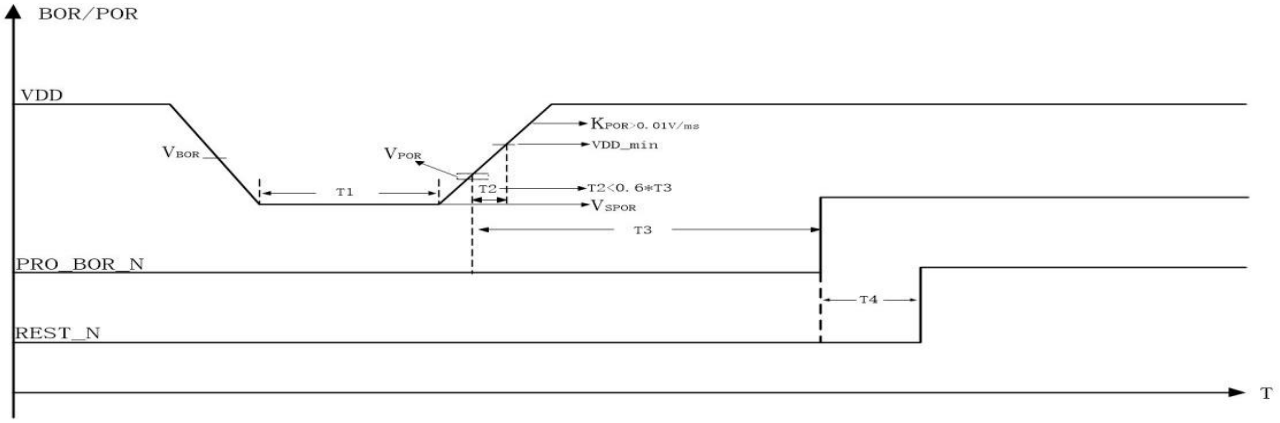


Reset timing diagram

Reset sequence description:

1. The chip has a power-on reset, and the analog POR module delays for 93ms, and po_n is pulled high.
2. The programmer sends instructions to make the chip enter the programming mode (prog_en is pulled high), and the system is in a global reset state in the programming mode. After the programming is completed, the programming mode is exited. After a delay of 20ms, rst_n is pulled high and the chip enters normal operation.
3. During normal operation, any one of watchdog reset, address overflow reset, and soft reset occurs, rst_n is pulled low, after a delay of 20ms, rst_n is pulled high, and the chip enters normal operation.
4. In debug mode, configure debug reset, pull down rst_n, pull up 1 system clock in debug_rst_out_n, pull up rst_n, and the chip enters normal operation.

Power-up/power-down sequence:



Power-on reset diagram

BOR/POR Parameters:

Symbol	Parameter	Min	Typ	Max	Unit
VSPOR	Power on reset start voltage	-	-	300	mV
KPRO	Power on reset voltage rate	0.01	-	-	V/ms
VPOR	Power on reset voltage	1.1	1.5	2.2	V
VBOR	Brownout reset voltage (±10%), hysteresis 0.2V	-	VBOR	-	V
VDD_min	Minimum operating voltage	2.7	-	-	V
T1	VDD keep VSPOR time	0.1	-	-	ms
T2	VPOR from VDD_min time	-	-	0.6*T3	ms
T3	Reset POR_BOR_N duration	55	93	131	ms
T4	Global reset effective time	-	20	-	ms

Note: VBOR voltage is selected by register BOR_SEL[2:0].

When VDD is affected by the load or severely disturbed, if the voltage drops into the voltage dead zone and the chip is not within the working voltage range, it may cause the system to work abnormally, such as EEPROM-like data loss. The function of power-down reset (BOR) is to monitor when VDD drops to the BOR voltage, the MCU can generate a power-down reset in advance to avoid system errors.

Suggestions to prevent entering the voltage dead zone and reduce the probability of system error:

- BOR is turned on when the program is first initialized, and BOR is turned on without delay
- Increase the voltage drop slope

5.3.2. Reset System Register

SFR 寄存器				
地址	名称	读写	复位值	说明
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0xD7	RST_STAT	RW	x000_0010b	Reset flag register
0xFF	BOR_SEL	RW	xxx1_1000b	BOR control register

SOFT_RST(8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Software reset register. Software reset is only generated when the register value is 0x55.

RST_STAT (D7H) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	--	Reserved
6	DEBUG_F	0: No effect; 1: Trim configuration reset occurred
5	SOFT_F	0: No effect; 1: Software reset occurred
4	PROG_F	0: No effect; 1: A programming reset occurred
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred
2	BO_F	0: No effect; 1: Power-down reset occurred
1	PO_F	0: No effect; 1: Brown-out reset occurred
0	WDTRST_F	0: No effect; 1: Watchdog timer overflow reset occurred

Power-on reset RST_STAT register reset value 0x02; other mode reset: the reset flag bit

corresponding to the RST_STAT register is 1, other reset flag bits keep their original state.

BOR_SEL(FFH) BOR control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	PD_BOR	SEL_BOR_DELAY	SEL_BOR_VTH		
R/W	-	-	-	R/W	R/W	R/W		
Reset value	-	-	-	1	1	0		

Bit number	Bit symbol	Description
4	PD_BOR	BOR control register 1: close; 0: open, close by default Note: It is recommended to open BOR without delay when the program is first initialized
3	SEL_BOR_DELAY	Select the signal, select the power-down delay of BOR 0: Delay time 1; 1: Delay time 2
2~0	SEL_BOR_VTH	BOR threshold selection 000: reserved; 001: 2.8V; 010: 3.3V; 011: 3.7V; 1xx: 4.2V

BOR_SEL register is connected to power-on reset: state is 0x18, other resets will not change the configuration value.

Delay selection SEL_BOR_DELAY	SEL_BOR_VTH	BOR			
		Power down threshold (V)	Recovery threshold (V)	Hysteresis (V)	Delay (μs)
0	000	-	-	-	-
	001	2.8	2.9	0.1	83.9
	010	3.3	3.4	0.1	97.6
	011	3.7	3.8	0.1	107.2
	1XX	4.2	4.3	0.1	117.2
1	000	-	-	-	-
	001	2.8	2.9	0.1	167.8
	010	3.3	3.4	0.1	195.7
	011	3.7	3.8	0.1	215.1
	1XX	4.2	4.3	0.1	235.4

5.4. Working Mode

The BF7412AMXX-XJLX series has 3 working modes, which can be selected according to different situations.

The BF7412AMXX-XJLX provides the SYS_CLK_CFG register, whose Bit2 can be configured to control the MCU into WAIT mode. The BF7412AMXX-XJLX provides the PCON register, the Bit0 of which can be configured to control the MCU into low power mode.

- **Active mode**

That is, the normal working mode, the modules keep working normally, and the functions of each module are controlled by the software configuration.

- **Wait mode**

Enter Wait mode by writing 1 to SYS_CLK_CFG.2. Core related modules and PWM0 ~2 modules do not work, other modules can work and exit this mode by interrupt.

- **Low_power mode**

Enter low power mode by writing 1 to PCON.0. RC1M and PLL off, LIRC working, WDT/Timer2 configurable working. CPU and other digital modules are not working.

SYS_CLK_CFG (84H) Clock control register

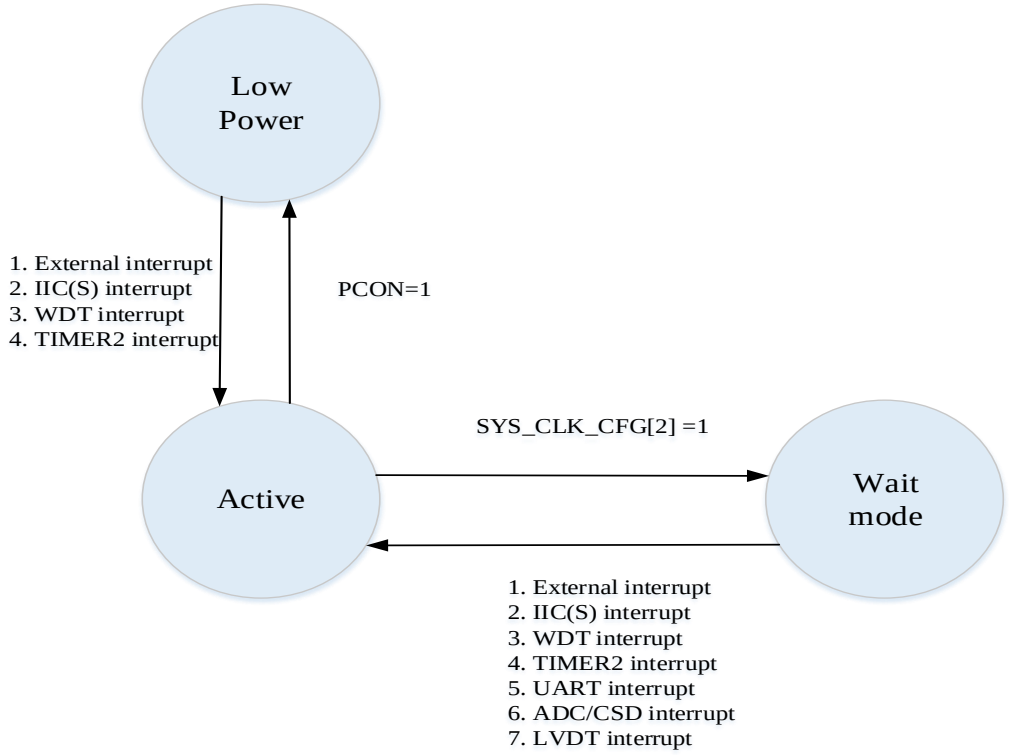
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WAIT_MODE	PLL_CLK_SEL	
R/W	-	-	-	-	-	R/W	R/W	
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
2	WAIT_MODE	WAIT mode enable 1: The chip enters WAIT mode; 0: The chip exits WAIT mode

PCON(87H) Low-power mode select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-		LPM
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	LPM	Low power mode control 1: Low power consumption mode; 0: Normal mode, automatically cleared after waking up Note: After waking up, the software delay must be ≥100μs, otherwise the wake-up function is abnormal



Working mode conversion diagram

Ways to exit Wait mode:

- Enable any one of IIC, External Interrupt0, External Interrupt1, External Interrupt2, External Interrupt3, WDT, Timer2, CSD, ADC, LVDT, UART can wake up the chip, exit the Wait mode, and the CPU executes the interrupt service routine.

Ways to exit Low_power mode:

- Enable IIC, External Interrupt0, External Interrupt1, External Interrupt2, External Interrupt3, WDT, Timer2, any of them can wake up the chip and exit the Low_power mode. After the interrupt response is generated, the CPU executes the interrupt service routine related to the interrupt vector. And after the RETI return instruction is executed, it returns to the next instruction that causes the CPU to enter the Low_power mode to continue running the program.

Note: PCON = 0x01, BOR off can obtain lower power consumption, but the chip needs to ensure that it is in the normal operating voltage range (2.7V~5.5V), if the chip power supply is unstable, resulting in less than 2.7V, it is strongly recommended that BOR be turned on.

Mode	Contions for entering this mode	Effect on the clock	
Active/Wait	PCON=0	LIRC	work
		XTAL32K	Depends on software configuration
		RC1M	work
		PLL	work
Low Power	PCON=1	LIRC	work
		XTAL32K	Depends on software configuration
		RC1M	close
		PLL	close

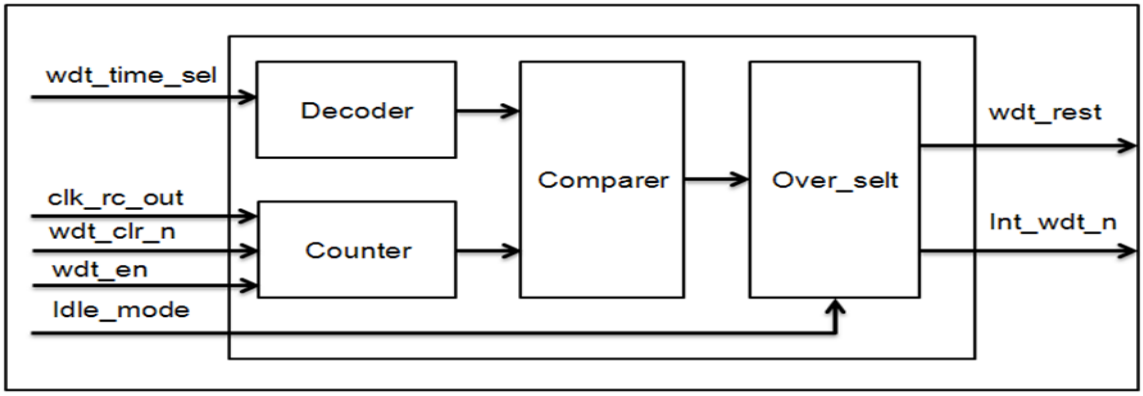
Working status table of clock source in each mode

NO	Module Name	Clock source	Work status		
			Active	Wait	Low Power
1	s8051	F_sys_clk	√	×	×
2	UART0~1	PLL_24M	According Configuration	According Configuration	×
3	PWM0~2	PLL_24M	According Configuration	×	×
4	Internal Timer0	F_sys_clk	According Configuration	×	×
5	Internal Timer1	F_sys_clk	According Configuration	×	×
6	External Timer2	LIRC/ XTAL32K	According Configuration	According Configuration	According Configuration
7	WDT	LIRC	According Configuration	According Configuration	According Configuration
8	ADC_CTRL	PLL_48M	According Configuration	According Configuration	×
9	CSD_Timing	PLL_48M	According Configuration	According Configuration	×
10	IIC(S)	F_sys_clk	According Configuration	According Configuration	According Configuration

Status table for each digital module in different modes

5.5. WDT

The WDT timing counting circuit uses the internal low-speed clock LIRC for timing, and the configurable timing time is 2^n*18ms (n=0,1,2,3,4,5,6,7)----- Here n is the configuration value of the timing configuration register.



Classification of WDT overflow signals due to the particularity of the system applications:

In normal mode, if the WDT overflow occurs, the overflow signal is the WDT overflow reset signal, the WDT overflow reset affects the global reset. At this point, the system implements a global reset action and reloads the configuration information.

In Low_power mode, if the WDT overflow, the overflow signal is the WDT interrupt signal. Interrupt wake-up chip exits Low_power mode and executes WDT interrupt service function.

The watchdog module is a timing counting module. Its count clock is the internal low-speed clock LIRC. Its timing clear signal is composed of global reset and configuration clear. This signal is synchronously released by the watchdog timing clock in the reset module; The clearing action is generated every time the CPU configures the watchdog timer configuration register (WDT_CTRL), and the watchdog restarts timing; at the same time, the watchdog counter has the watchdog count enable control, when the count enable is valid, After the watchdog generates a timing overflow (reset or interrupt), as long as the watchdog counting enable is not turned off, the watchdog counter will restart counting.

5.5.1.WDT Related Registe

SFR register				
Address	**Address**	**Address**	**Address**	**Address**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timeout configugration register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

WDT SFR list

5.5.2.WDT Register Detailed Description

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status, set 0, write WDT_CTRL can set 0. 1: interrupt effective 0: invalid interrupt

WDT_CTRL(91H) WDT timing overflow control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~0	WDT_TIME_SEL	WDT overflow timer register. Timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

The watchdog uses the internal low-speed clock LIRC to complete the timing function and can achieve timing from 18ms to 2.3s. The timing length is controlled by SFR (WDT_CTRL), as shown in the following table

WDT_EN(92H) WDT timing enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Turn off WDT when writing 0x55, write other values to enable WDT, the WDT always works after the reset is over. Clearing the WDT is done by writing to the WDT_CTRL register. Whichever values is written to this register will clear the WDT.

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: there is a WDT/Timer2 interrupt flag; 0: no WDT/Timer2 interrupt flag

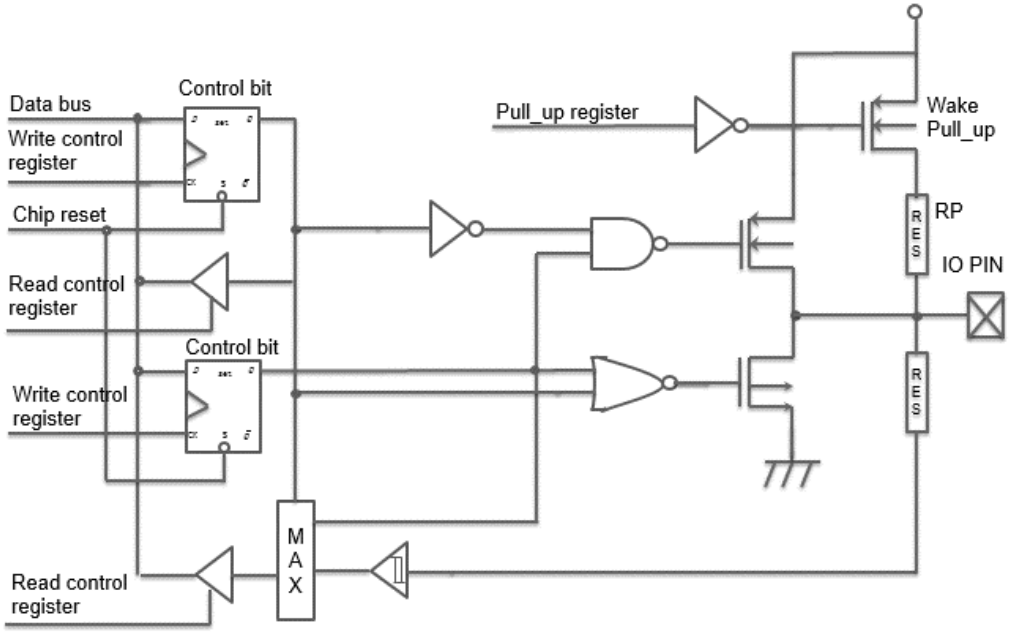
IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

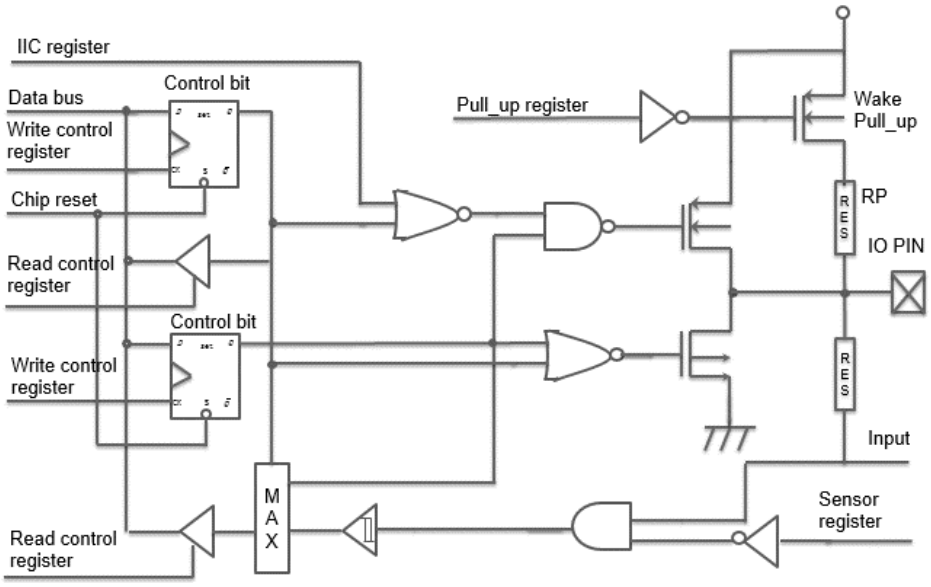
Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority

6. GPIO

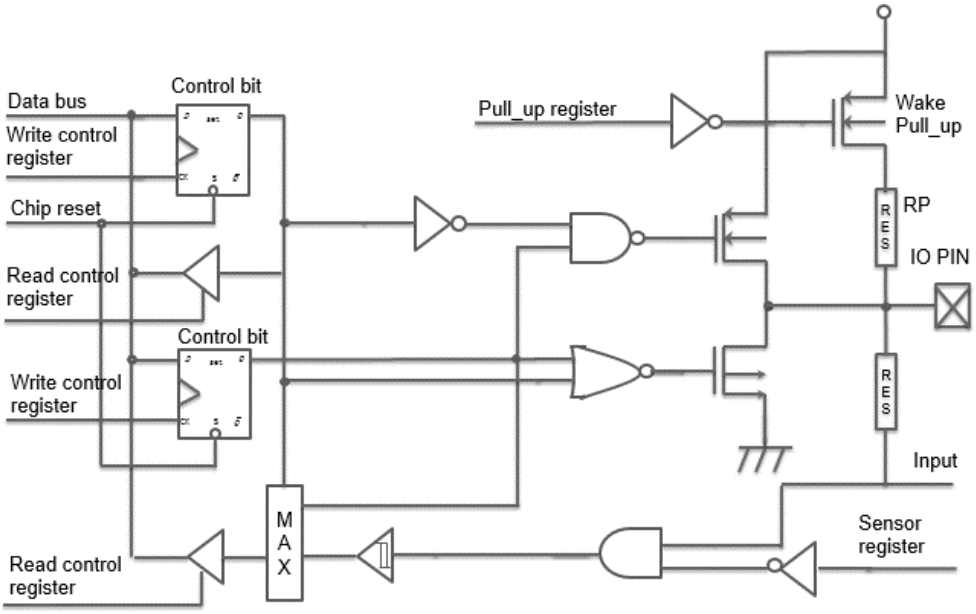
Some pins of the GPIO port are multiplexed with device peripheral functions, and cannot be configured as multiple clock functions at the same time, otherwise it will cause malfunction. IIC communication port, open-drain output, pull-up resister required.



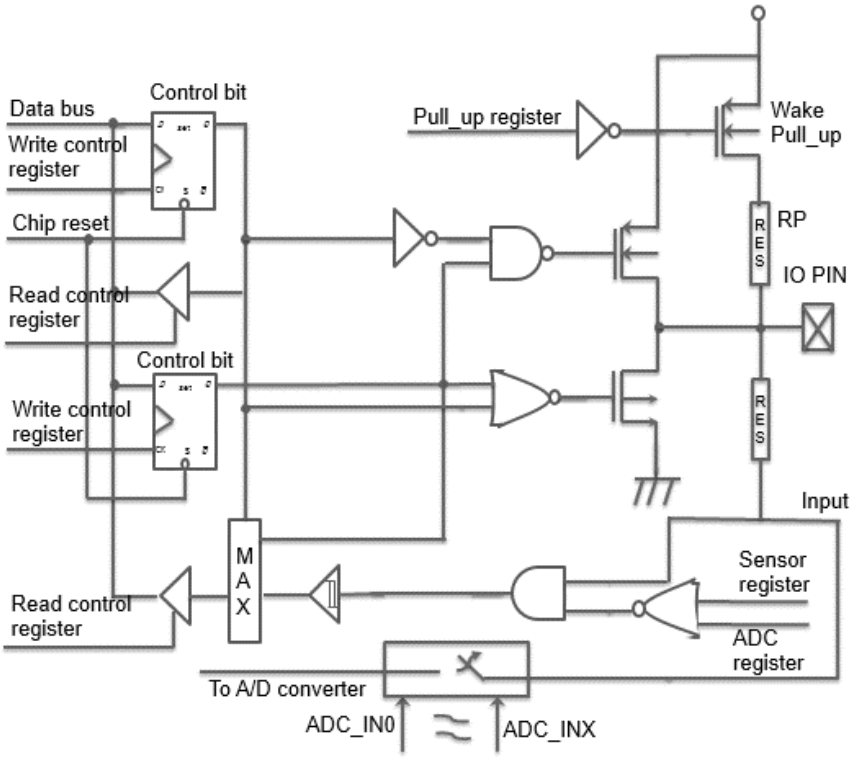
General IO structure



Open-drain output structure



SNS IO structure



ADC IO structure

TRISX register (Direction Register): TRISX set to 1 can be configured as input pin, set to 0 can be configured as output pin.

DATAX register (Data Register): DATAX set to 1 the data in DATAX will be configured as high, set to 0 the data in DATAX will be configured as low.

PU_PX register (Pull-up resistance enable register): PU_PX set to 1 corresponding pin pull-up

resistor enable, clear the corresponding pin does not enable pull-up resistor, and pull-up resistor 4.7k(PB port pull-up resistor 28k).

PD_PB register (PB pull-down resistor enable register): Set PD_PB to 1 to enable the corresponding pin pull-down resistor, clear the corresponding pin to disable the pull-down resistor, built-in pull-down resistor 28k.

ODRAIN_EN register: ODRAIN_EN set to 1 corresponding pin will enable open drain output, set to 0 corresponding pin corresponding pin output disenabled, automatically turn on open-drain after enabling IIC function. IIC/UART recommends using external pull-up resistors.

Supports 8 GPIO ports for high current drive functions.

6.1. GPIO Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0xF8	DATAA	RW	xxxx_xx11b	PA data register
0x80	DATAB	RW	1111_1111b	PB data register
0x90	DATAC	RW	1111_1111b	PC data register
0x98	DATAD	RW	1111_1111b	PD data register
0xD8	PD_PB	RW	0000_0000b	PB port pull-down resistor enable register
0xDD	PU_PA	RW	xxxx_xx00b	PA port pull-up resistor enable register
0xDE	PU_PB	RW	0000_0000b	PB port pull-up resistor enable register
0xDF	PU_PC	RW	0000_0000b	PC port pull-up resistor enable register
0xE2	PU_PD	RW	0000_0000b	PD port pull-up resistor enable register
0xEA	TRISA	RW	xxxx_xx11b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_1111b	PC direction register
0xED	TRISD	RW	1111_1111b	PD direction register
0xEE	COM_IO_SEL	RW	0000_0000b	COM port selection configuration register
0xEF	ODRAIN_EN	RW	xxxx_x000b	PA0/PA1/PD6 port open drain enable register

Port configuration SFR list

6.2. GPIO Register Detailed Description

6.2.1. Data Register

DATAA (F8H) PA data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PA1	PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA data register. The output level of the PA group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

DATAB(80H)PB data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PBdata register. The output level of the PB group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

DATAC(90H) PC data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register. The output level of the PC group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

DATAD(98H) PD data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD data register. The output level of the PD group can be configured as the GPIO port. The read value is the level state of the current IO port (input) or the configured output (output) value.

6.2.2. Pull-up Resistor Enable Register

PU_PA (DDH) PA port pull-up resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	PU_PA1	PU_PA0
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	--	Port PA pull-up resistor enable register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PB(DEH) PB port pull-up resisor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PB port pull-up resisor enable register. Set PU_PB to 1 to enable the corresponding pin pull-up resistor, clear the corresponding pin to disable the pull-up resistor, the pull-up resistor is 4.7K.

PU_PC(DFH) PC port pull-up resisor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PCport pull-up resisor enable register. Set PU_PC to 1 to enable the corresponding pin pull-up resistor, clear the corresponding pin to disable the pull-up resistor, the pull-up resistor is 4.7K.

PU_PD (E2H) PD port pull-up resisor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PD port pull-up resisor enable register. Set PU_PD to 1 to enable the corresponding pin pull-up resistor, clear the corresponding pin to disable the pull-up resistor, the pull-up resistor is 4.7K.

6.2.3. Direction Register

TRISA (EAH) PA port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	1

Bit number	Bit symbol	Description
1~0	--	PA direction register, 0: output; 1: input

TRISB(EBH) PB port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB direction register, 0: output; 1: input

TRISC(ECH) PC port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC direction register 0: output; 1: input

TRISD(EDH) PD port direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PD direction register 0: output 1: input

6.2.4. Large Current Sink

COM_IO_SEL (EEH) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	COM port selection configuration register, PB port corresponds to bit selection 1: Select the COM port mode and turn on the high current function; 0: select IO port mode

6.2.5. Open Drain Output Enable Register

ODRAIN_EN (EFH) PA0/PA1/PD6 port open drain enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	--	PA0/PA1/PD6 open-drain output enable register Bit[0]: PA0, Bit[1]: PA1, Bit[2]: PD6 1: Open drain output; 0: CMOS output

6.2.6. Pull-down Resistor Enable Register

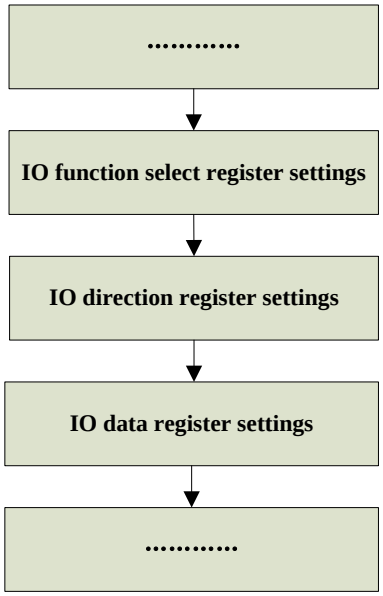
PD_PB(D8H) PB port pull-down resistor enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	PD_PB7	PD_PB6	PD_PB5	PD_PB4	PD_PB3	PD_PB2	PD_PB1	PD_PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	PD_PBn (n=7~0)	PB port pull-down resistor enable register 1: The pull-down resistor is enabled; 0: The pull-down resistor is not enabled

6.3. GPIO Configuration Process

When setting the port to GPIO, the following three sets of registers need to be set accordingly.



IO configuration flow chart

Notes:

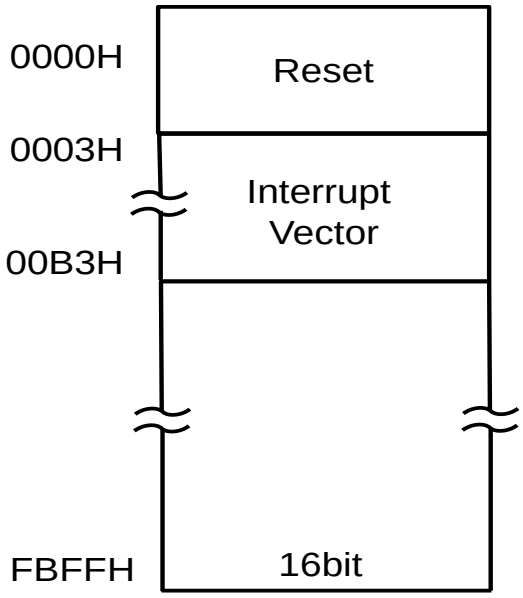
The default source current drive capability of the IO port is typically 20mA, the sink current drive capability typically 35mA @5V 0.9VCC.

7. Interrupt

7.1. Interrupt Sources and Entry Address

Interrupt source	Condition	Sign	Enable control	Priority control	Interrupt vector	Query priority	Interrupt number	Flag removal method	Low power wake
INT0	External interrupt 0 condition is met	IE0	IEN0[0]	IPL0[0]	0x0003	1	0	User must clear	Yes
Timer0	Timer0 overflow	TF0	IEN0[1]	IPL0[1]	0x000B	2	1	User must clear	No
INT1	External interrupt 1 condition is met	IE1	IEN0[2]	IPL0[2]	0x0013	3	2	User must clear	Yes
Timer1	Timer1 overflow	TF1	IEN0[3]	IPL0[3]	0x001B	4	3	User must clear	No
INT2	External interrupt 2 condition is met	IE2	IEN1[2]	IPL1[2]	0x004B	5	9	User must clear	Yes
IIC	Accept or send completed	IE3	IEN1[3]	IPL1[3]	0x0053	6	10	User must clear	Yes
ADC	ADC conversion completed	IE4	IEN1[4]	IPL1[4]	0x005B	7	11	User must clear	No
CSD	Counter overflow	IE5	IEN1[5]	IPL1[5]	0x0063	8	12	User must clear	No
INT3	External interrupt 3 condition is met	IE6	IEN1[6]	IPL1[6]	0X006B	9	13	User must clear	No
WDT/ Timer2	WDT/Timer2 overflow	IE7	IEN1[7]	IPL1[7]	0x0073	10	14	User must clear	Yes
LVDT	Voltage conditions meet	IE8	IEN2[0]	IPL2[0]	0x007B	11	15	User must clear	No
UART0	Accept or send completed	IE9	IEN2[1]	IPL2[1]	0x0083	12	16	User must clear	No
UART1	Accept or send completed	IE10	IEN2[2]	IPL2[2]	0x008B	13	17	User must clear	No

List of interrupt information



When the chip generates a reset signal, the program starts from the 0x0000 address. When an interrupt signal occurs, the program will jump to the interrupt vector program address to execute the interrupt service routine.

7.2. Interrupt Function

7.2.1. Interrupt Response

When an interrupt request, CPU according to the interrupt vectors determine the type of interrupt service routine (ISR) to run. CPU complete execution ISR, unless a higher priority interrupt source applying for a break. After each ISR has RETI (return from interrupt) instruction. After RETI instruction, CPU continues to execute the program before the interrupt did not happen.

ISR can only be a higher priority interrupt request interrupt. That is, the low-priority ISR can be interrupted by a high-priority interrupt request.

The BF7412AMXX-XJLX responses interrupt request until the current instruction finished. If the RETI instruction is being executed or read IPL, IEN register, after an additional instruction then respond the interrupt request.

7.2.2. Interrupt Priority

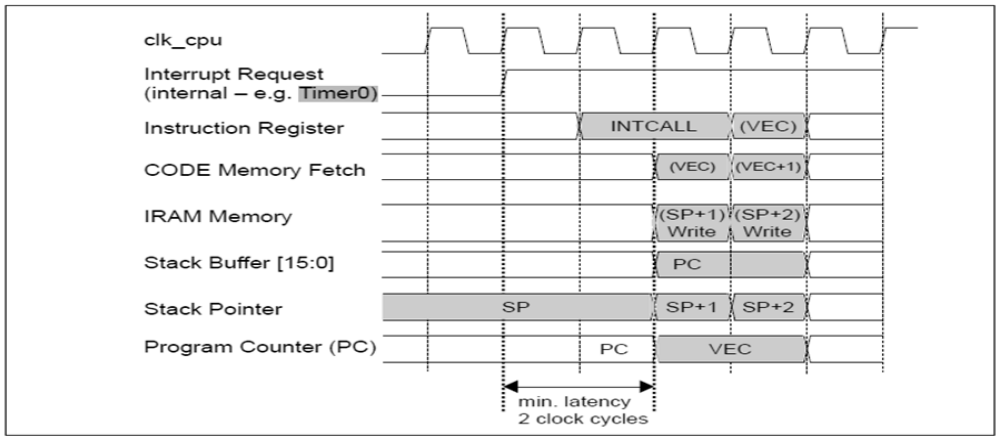
The BF7412AMXX-XJLX has two interrupt priority levels: interrupt level and default priority. Interrupt levels (highest, high, and low) take precedence over the default priority. The priority set to high is the first to respond. When the priority is set to the same level, the response will be queued by default. If allowed, the power-down interrupt is the only highest-level interrupt source. Other interrupt sources can be set to high priority or low priority.

Each interrupt source can be assigned a priority level (high or low), and the default priority. The same level of interrupt sources (such as both high priority) the priority is the default priority decision. Interrupt service routine in progress can only be a high-priority interrupt request interrupt.

7.2.3. Interrupt Sampling

Internal modules such as internal timers and serial ports generate interrupt requests through interrupt flag bits in their respective SFRs. At the end of first clock per instruction cycle (C1), at the rising edge of the external interrupt system clock sampling.

To ensure edge-triggered interrupt is detected, the corresponding port must maintain high level for two clocks and maintain low for level two clock.



Interrupt sampling timing diagram

7.2.4. Interrupt Wait

Interrupt response time is determined by current state. Fastest response time is five instruction cycles: one cycle to detect the interrupt request, the other 4 used to execute long call (LCALL) to ISR.

When the system is executing a RETI instruction and is followed by a MUL or DIV instruction, the interrupt waits for the longest time (13 instruction cycles). This 13 instruction cycles are as follows: one cycle to detect the interrupt request, three to complete the RETI, five used to execute DIV or MUL instruction, 4 used to execute long call (LCALL) to ISR. In this case, the response time is 13 clock cycles.

7.3. Interrupt Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/LVDT buck interrupt status register
0x88	TCON	RW	0000_0x0xb	Timer control register
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xC2	PERIPH_IO_SEL3	RW	x000_0000b	INT3 select enable register 3
0xC3	PERIPH_IO_SEL2	RW	0000_0000b	INT3 select enable register 2
0xC4	PERIPH_IO_SEL1	RW	0000_0000b	INT3 select enable register 1
0xE1	IRCON2	RW	xxxx_x000b	Interrupt flag register 2
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	xxxx_x000b	Interrupt enable register 2
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF4	IPL2	RW	xxxx_x000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	EXT_INT_CON	RW	x001_0101b	External interrupt polarity control register

Interrupt SFR list

7.3.1. Interrupt SFR Detailed Description

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_WDT_STAT	WDT interrupt status, set 0, write WDT_CTRL can set 0. 1: interrupt effective 0: invalid interrupt
0	INT_TIMER2_STAT	TIMER2 interrupt status, set 0, write TIMER2_CFG can set 0. 1: interrupt effective 0: invalid interrupt

INT_POBO_STAT (86H) LVDT boost/LVDT buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	Lvdt boost interrupt status 1: boost interrupt is valid 0: boost interrupt is invaild
0	INT_BO_STAT	Lvdt buck interrupt state 1: buck interrupt is valid 0: buck interrupt is invalid

TCON(88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
3	IE1	External interrupt 1. The hardware set 1, the software is cleared.
1	IE0	External interrupt 0. The hardware set 1, the software is cleared

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer1 interrupt enable bit 0: Disable timer 1 to apply for interrupt;

		1: Allow timer 1 flag bit to apply for interrupt.
2	EX1	INT_EXT1 enable bit 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 interrupt enable bit 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1(Timer1 interrupt) priority selection bit. 0: TF1(Timer1 interrupt) is low priority. 1: TF1(Timer1 interrupt) is high priority.
2	PX2	INT_EXT1 interrupt priority selection bit. 0: INT_EXT1 is low priority. 1: INT_EXT1 is high priority.
1	PT0	TF0(Timer0 interrupt) priority selection bit. 0: TF0(Timer0 interrupt) is low priority. 1: TF0(Timer0 interrupt) is high priority.
0	PX0	INT_EXT0 interrupt priority selection bit. 0: INT_EXT0 is low priority. 1: INT_EXT0 is high priority.

PERIPH_IO_SEL3(C2H) INT3 select enable register 3

Bit number	7	6	5	4
Symbol	–	INT3_22_IO_SEL	INT3_21_IO_SEL	INT3_20_IO_SEL
R/W	–	R/W	R/W	R/W
Reset value	–	0	0	0
Bit number	3	2	1	0
Symbol	INT3_19_IO_SEL	INT_3_18_IO_SEL	INT3_17_IO_SEL	INT3_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6~0	INT3_n_IO_SEL (n=22~16)	INT3_n port selection enable 1: Select INT function; 0: Do not select INT function

PERIPH_IO_SEL2(C3H) INT3 select enable register 2

Bit number	7	6	5	4
Symbol	INT3_15_IO_SEL	INT3_14_IO_SEL	INT3_13_IO_SEL	INT3_12_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_11_IO_SEL	INT3_10_IO_SEL	INT3_9_IO_SEL	INT3_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=15~8)	INT3_n port selection enable 1: Select INT function; 0: Do not select INT function

PERIPH_IO_SEL1(C4H) INT3 select enable register 1

Bit number	7	6	5	4
Symbol	INT3_7_IO_SEL	INT3_6_IO_SEL	INT3_5_IO_SEL	INT3_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT3_3_IO_SEL	INT3_IO_2_SEL	INT3_1_IO_SEL	INT3_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT3_n_IO_SEL (n=7~0)	INT3_n port selection enable 1: Select INT function; 0: Do not select INT function

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IE10	IE9	IE8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description

7~3	--	Reserved
2	IE10	UART1 interrupt flag 1: There is a UART1 interrupt flag; 0: No UART1 interrupt flag
1	IE9	UART0 interrupt flag 1: There is a UART0 interrupt flag; 0: No UART0 interrupt flag
0	IE8	LVDT interrupt flag 1: There is a LVDT interrupt flag; 0: No LVDT interrupt flag

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable
6	EX6	External interrupt 3 interrupt enable 1: Interrupt enable; 0: Interrupt disable
5	EX5	CSD interrupt enable 1: interrupt enable; 0: interrupt disable
4	EX4	ADC interrupt enable 1: interrupt enable; 0: interrupt disable
3	EX3	IIC interrupt enable 1: interrupt enable; 0: interrupt disable
2	EX2	External interrupt 2 interrupt enable 1: interrupt enable; 0: interrupt disable
1~0	-	Reserved

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	EX10	EX9	EX8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~3	-	Reserved
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable
0	EX8	LVDT interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: There is a WDT/Timer2 interrupt flag; 0: No WDT/Timer2 interrupt flag
6	IE6	External interrupt 3 interrupt flag 1: There is a External interrupt 3interrupt flag; 0: No External interrupt 3 interrupt flag
5	IE5	CSD interrupt flag 1: There is a CSD interrupt flag; 0: No CSD interrupt flag
4	IE4	ADC interrupt flag 1: There is a ADC interrupt flag; 0: No ADC interrupt flag
3	IE3	IIC interrupt flag 1: There is a IIC interrupt flag; 0: No IIC interrupt flag
2	IE2	External interrupt 2 interrupt flag 1: There is a INT2 interrupt flag; 0: No INT2 interrupt flag
1~0	–	Reserved

PERIPH_IO_SEL (F2H) IIC /INT function control register

Bit number	7	6	5	4	3

Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	IIC_IO_SEL	
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	1	0	0	0
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		
Reset value	0	0	0		

Bit number	Bit symbol	Description
2	INT2_IO_SEL	INT2 select enable, correspond PD7 1: select INT2 function 0: not select INT2 function
1	INT1_IO_SEL	INT1 select enable, correspond PD6 1: select INT1 function 0: not select INT1 function
0	INT0_IO_SEL	INT0 select enable, correspond PD0 1: select INT0 function 0: not select INT0 function

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	IPL2.2	UART1 interrupt priority. 0: low priority; 1: high priority
1	IPL2.1	UART0 interrupt priority. 0: low priority; 1: high priority
0	IPL2.0	LVDT interrupt priority. 0: low priority; 1: high priority

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description

7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority
6	IPL1.6	External interrupt 3 interrupt priority. 0: low priority; 1: high priority
5	IPL1.5	CSD interrupt priority. 0: low priority; 1: high priority
4	IPL1.4	ADC interrupt priority. 0: low priority; 1: high priority
3	IPL1.3	IIC interrupt priority. 0: low priority; 1: high priority
2	IPL1.2	External interrupt 2 priority. 0: low priority; 1: high priority
1~0	--	Reserved

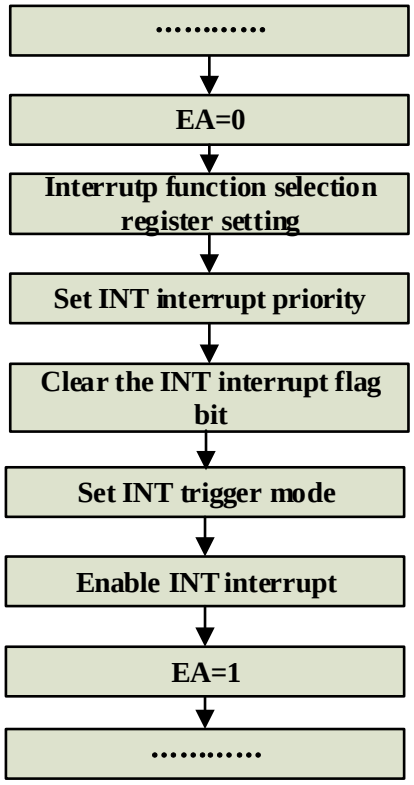
EXT_INT_CON (F7H) External interrupt polarity control register

Bit number	7	6	5	4
Symbol	-	INT3_POLARITY	INT2_POLARITY	
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1
Bit number	3	2	1	0
Symbol	INT1_POLARITY		INT0_POLARITY	
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1

Bit number	Bit symbol	Description
6	INT3_POLARITY	External interrupt 3_x trigger polarity selection: 1: Rising edge (high level wake-up in low power mode) 0: Falling edge (low-level wake-up in low-power mode)
5~4	INT2_POLARITY	External interrupt 2 trigger polarity selection: 01: Falling edge (low-level wake-up in low-power mode) 10: rising edge (high level wake-up in low power mode) 00/11: Double edge (low-level wake-up in low-power mode)
3~2	INT1_POLARITY	External interrupt 1 trigger polarity selection: 01: Falling edge (low-level wake-up in low-power mode) 10: rising edge (high level wake-up in low power mode) 00/11: Double edge (low-level wake-up in low-power mode)
1~0	INT0_POLARITY	External interrupt 0 trigger polarity selection: 01: Falling edge (low-level wake-up in low-power mode) 10: rising edge (high level wake-up in low power mode) 00/11: Double edge (low-level wake-up in low-power mode)

Note: INT3 shares an interrupt vector and can only respond to one external interrupt at the same time. When the multi-channel pin external interrupt rising edge or falling edge trigger is enabled, all the enabled external interrupt pins must be released during the detection process to respond to the current trigger signal (when the falling edge is triggered, the release is high. When the rising edge is triggered, the release is low).

7.4. External Interrupt Configuration Process



INT0/1/2/3 configuration process chart

8. Timer

The BF7412AMXX-XJLX contains three Timers (Timer0/Timer1/Timer2). Each Timer contains a 16-bit register that appears as two bytes when accessed: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). Timer2 register is low byte TIMER2_SET_L, high byte TIMER2_SET_H.

Timer features:

- 2 16-bit Timers, 1 32-bit Timer;
- Timer0 connection system clock, partial frequency within the clock F_sys_clk/12;
- Timer1 connection system clock, partial frequency within the clock F_sys_clk/12;
- Timer2 optional internal RC or external crystal clock, frequency 32768Hz;
- Timer0 support 8-bit auto-reload timing, 16-bit manual reload timing function;
- Timer1 support 8-bit a auto-reload timing, 16-bit manual reload timing function;
- Timer2 support 32-bit automatic reload timing and manual reload timing, support interrupt wake-up function.

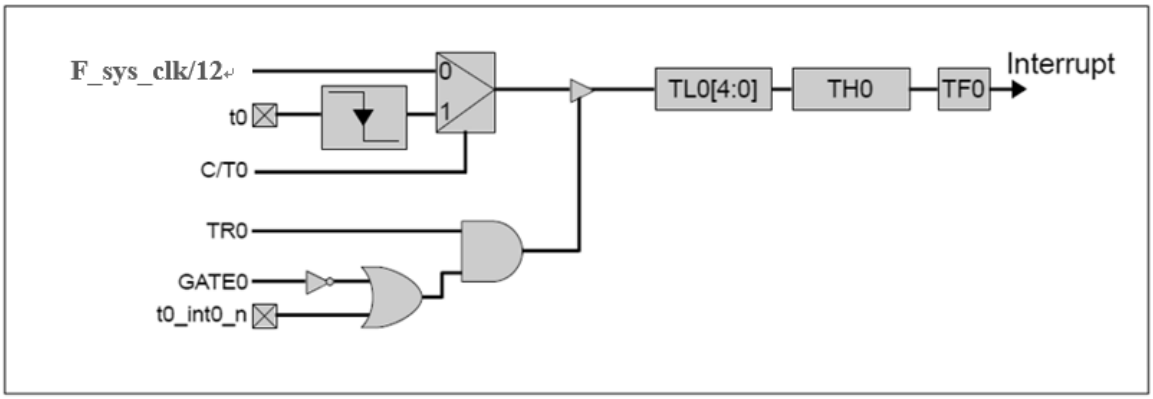
8.1. Timer0 and Timer1

The Timer 0/1 has four operating modes, controlled by TMOD SFR and TCON SFR. Timer0/1 four modes of operation as follows:

- Mode 0: 13-bit timer
- Mode 1: 16-bit timer
- Mode 2: 8-bit auto-reload timer
- Mode 3: Two 8-bit timers

In mode 0/1/2, timer 0 and timer 1 have exactly the same functions. In mode 3, timer 0 and timer 1 have different functions, and only timer 0 can set mode 3.

Mode 0：13-bit timer



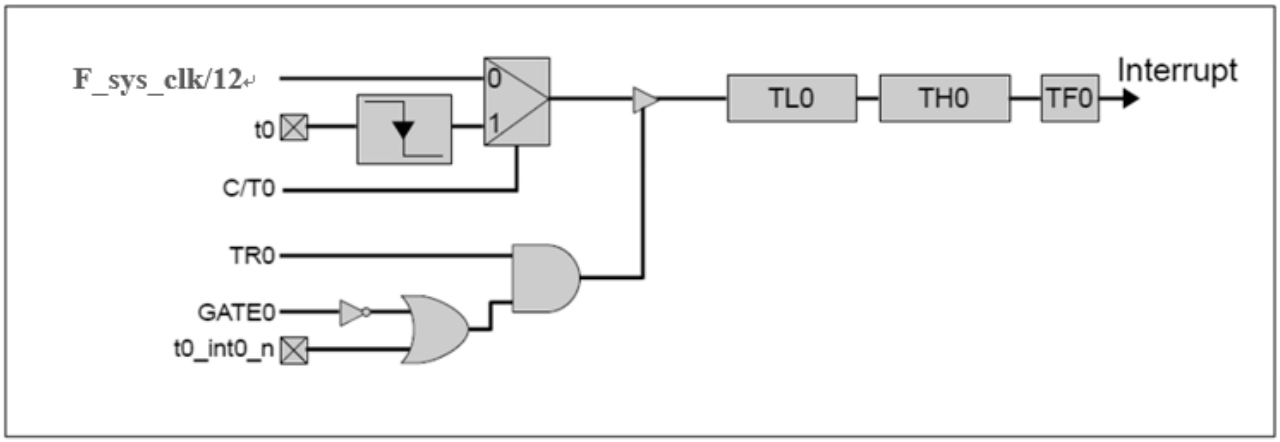
Mode 0 logical structure diagram

In mode 0, timer 0 and timer 1 work the same process, at the picture shows. In mode 0, Timer is 13bit counter, bit0-4 is TL0 (or TL1), other 8 bits is TH0 (or TH1). In TCON register (TR0/TR1)

to control timer0/1 start or stop.

The Timer counts the selected clock source(clk/12); When the 13bit counter counts up to all 1, the counter is cleared to 0(all 0) and TF0(or TF1)is set. In mode 0, TL0 (or TL1) high 3bit is not sure. These 3bit should be masked or ignored when reading the count value. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only TR0/1.

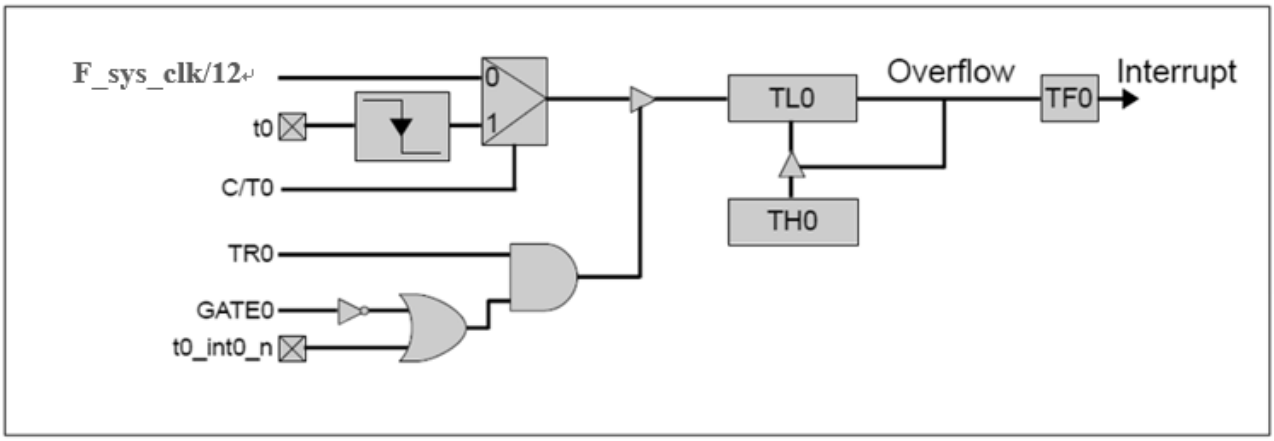
Mode 1: 16 bit timer



Mode 1 logical structure diagram

In mode 1, timer 0 and timer 1 work the same process. At the picture shows, in mode 1, Timer is 16bit counter, all 8 bits of the LSB register (TL0 or TL1) are used. When the counter count is accumulated to 0xFFFF, the counter is cleared to 0. In addition, mode 1 and mode 2 are the same. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only determined by TR0/1.

Mode2: 8-bit auto-reload timer

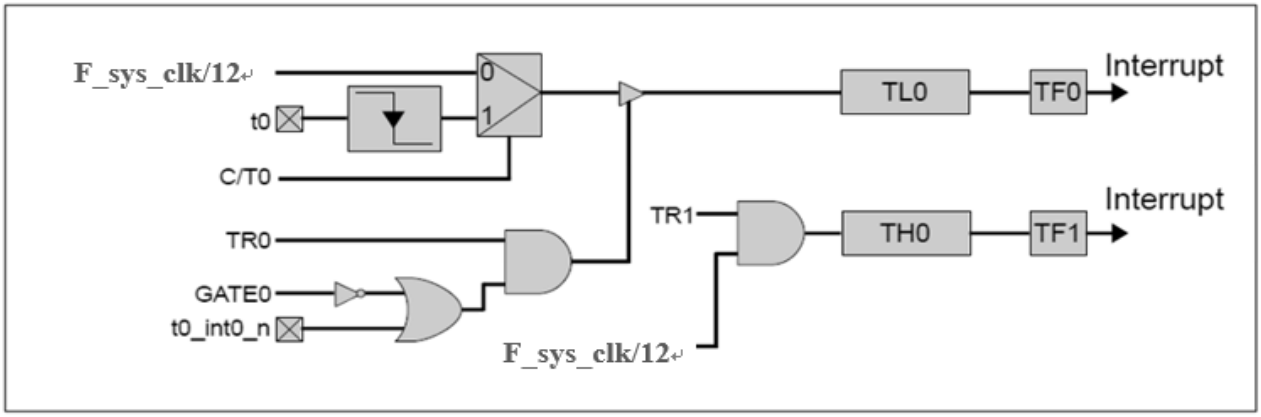


Mode 2 logical structure diagram

The modes of Timer0 and Timer1 are the same. In mode 2, the Timer is an 8bit counter with an automatic reload initial value. This counter is the LSB register (TL0 or TL1). The initial value that needs to be reloaded is saved in the MSB register (TL0 or TL1).

At the picture shows, mode 2 counter control is the same as mode 0 and mode 1. But in mode 2, When the TLn count is accumulated to FFh, the value stored in THn is overloaded to TLn. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only determined by TR0/1.

Mode3: Two 8-bit timers



Mode 3 logical structure diagram

In mode3, timer0 is two 8bit counter, then timer 1 stop count and save the value. Show as below, TL0 is an 8-bit register controlled by the control bit of Timer0. The counter uses GATE as the enable terminal to control the INT_EXT signal reception.

TH0 is a separate 8-bit counter. TH0 only used to count the clock cycle (12 division). Timer1 control bit and flag bit (TR1 and TF1) used as the TH0's control bit and flag.

When timer0 working in mode3, the use of Timer 1 is limited because Timer 0 uses the Timer 1 control(TR1) and interrupt flags(TF1). Timer 1 can still be used to generate baud rate. The value of TL1 and TH1 is still effective.

When timer0 working in mode 3, though mode control bit of Timer1 to control Timer1. In order to start timer1, need to set Timer 1 to mode 0, 1 or 2. Configure timer1 working in mode3, make timer1 stop. Timer 1 can be used as a Timer (clock is clk/12), However, since TR1 and TF1 are borrowed, overflow interrupts cannot be generated. When timer0 working in mode 3, timer1's GATE is effective. t0/t1, C/T0/CT1 all 0, t0_int0_n/t1_int1_n all 1, count enable is only determined by TR0/1.

8.1.1. Timer0/1 Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bits
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bits
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bits
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8 bits
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0

Timer0/1 SFR list

8.1.2. Timer0/1 Register Detailed Description

TCON(88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer1 overflow flag. Set to 1 when Timer1 overflows, or Timer0's TH0 overflows in mode three.
6	TR1	Timer1 start enable.When set to 1, enable the Timer1 count or Timer0 TH0 count in mode 3.
5	TF0	Timer0 overflow flag. The hardware set 1 when Timer0 overflows.
4	TR0	Timer0 start enable, when set to 1, start Timer0 count.

TMOD(89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer1 mode select bits 00=mode0 – 13-bit timer 01=mode1 – 16-bit timer 10=mode2 – 8-bit auto-reload timers 11=mode3 – Two 8-bit timers
1~0	M0[1:0]	Timer0 mode select bits 00=mode0 – 13-bit timer 01=mode1 – 16-bit timer 10=mode2 – 8-bit auto-reload timers 11=mode3 – Two 8-bit timers

TL0(8AH) Timer 0 counter low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TL1(8BH) Timer 1 counter 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH0(8CH) Timer 0 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

TH1(8DH) Timer 1 counter high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

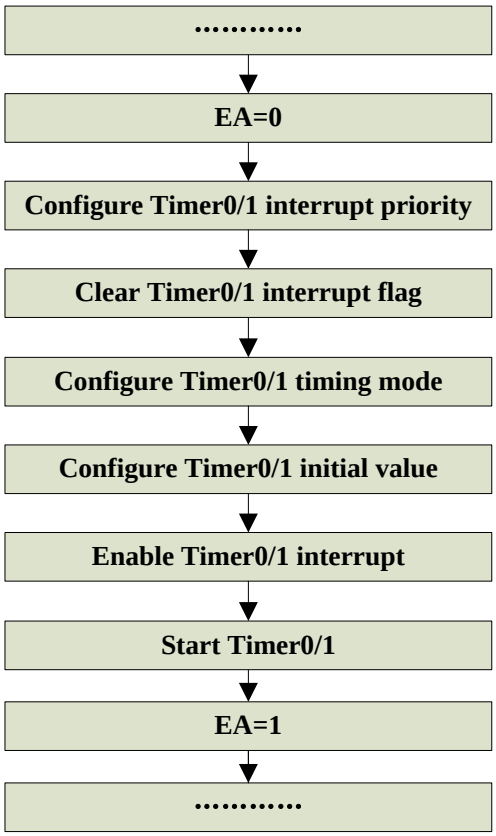
Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
3	ET1	Timer1 interrupt enable bit 0: Disable timer 1 to apply for interrupt; 1: Allow timer 1 flag bit to apply for interrupt.
1	ET0	Timer 0 interrupt enable bit 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	PT1	TF1(Timer1 interrupt) priority selection bit. 0: TF1(Timer1 interrupt) is low priority. 1: TF1(Timer1 interrupt) is high priority.
1	PT0	TF0(Timer0 interrupt) priority selection bit. 0: TF0(Timer0 interrupt) is low priority. 1: TF0(Timer0 interrupt) is high priority.

8.1.3. Timer0/1 Configure Process



Timer0/1 configure process

8.2. Timer2

Timer2 module plays a timing role, the internal structure of the Timer2 module is a 32-bit counter. Timed function by counting the input clock, the counting principle of Timer2 is the accumulation counts to the set value. Timer2's count clock can be selected from the external XTAL clock and the internal RC clock. Timer2 has two working modes: signal time mode and automatic reload mode, regardless of the mode, the timing is completed and an interruption occurs.

TIMER2_EN configuration Timer2 function enable, TIMER2_RLD configuration automatic reload mode and manual reload mode. Timing time is determined by registers TIMER2_SET_L and TIMER2_SET_H. The time clock can choose LIRC and XTAL32768Hz, which is determined by the clock selection register. Timer2 support interrupt wake up in low_power mode, software clear interrupt flag is required in the interrupt handler.

Timer2 timing duration formula:

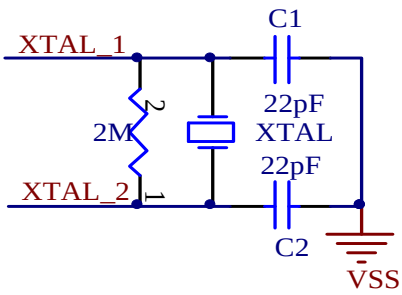
TIMER2_CNT_MOD=0:

$T_{TIMER2}=T_{TIMER2\_CLK}*(\{TIMER2\_SET\_H, TIMER2\_SET\_L\}+1)$

TIMER2_CNT_MOD=1:

$T_{TIMER2}=65536*T_{TIMER2\_CLK}*(\{TIMER2\_SET\_H, TIMER2\_SET\_L\}+1)$

Note: T_{TIMER2_CLK} = 1/32768 (s)



External crystal oscillator circuit reference

Notes:

1. **Arbitrary configuration TIMER2_SET_H, TIMER2_SET_L, TIMER2_CFG will clear counter;**
2. **External crystal oscillator circuit is for reference only, actual reference cryatal specifications.**

8.2.1. Timer2 Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0x85	INT_PE_STAT	RW	xxxx_xx00b	WDT/Timer2 interrupt status register
0x93	TIMER2_CFG	RW	xxxx_0000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 counter configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 counter configuration register, low 8 bits
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xxxx_0111b	Module switch control register

Timer2 registers list

8.2.2. Timer2 Register Detailed Description

INT_PE_STAT(85H)WDT/Timer2 interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_WDT_STAT	INT_TIMER2_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
0	INT_TIMER2_STAT	TIMER2 interrupt status, set 0, write TIMER2_CFG can set 0. 1: interrupt effective 0: invalid interrupt

TIMER2_CFG (93H) TIMER2 CFG register

Bit number	7~4	3	2	1	0
Symbol	-	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
3	TIMER2_CNT_MOD	TIMER2 count step mode select register 1: count step is 65536 clock. 0: count step is 1 clock.

2	TIMER2_CLK_SEL	TIMER2 clock select register 1: select XTAL32768Hz 0: select LIRC
1	TIMER2_RLD	TIMER2 reload enable control register 1: automatic reload mode 0: manual reload mode
0	TIMER2_EN	TIMER2 count enable register 1: turn on timing; 0: stop timing; In manual reload mode, the hardware automatically clears this register after timing is completed, stop count. In manual reload mode, will maintain the enable register after the count is completed. Automatically re-counting from 0, no matter which mode, configuring this register to 1 during counting will start counting from 0.

TIMER2_SET_H(94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_H[7:0]	TIMER2 count configuration register, high 8 bits. Configuring this register during the scan will recount.

TIMER2_SET_L(95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_L[7:0]	TIMER2 count configuration register, low 8 bits. Configuring this register during the scan will recount.

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2 interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2 interrupt flag 1: There is a WDT/Timer2 interrupt flag; 0: No WDT/Timer2 interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

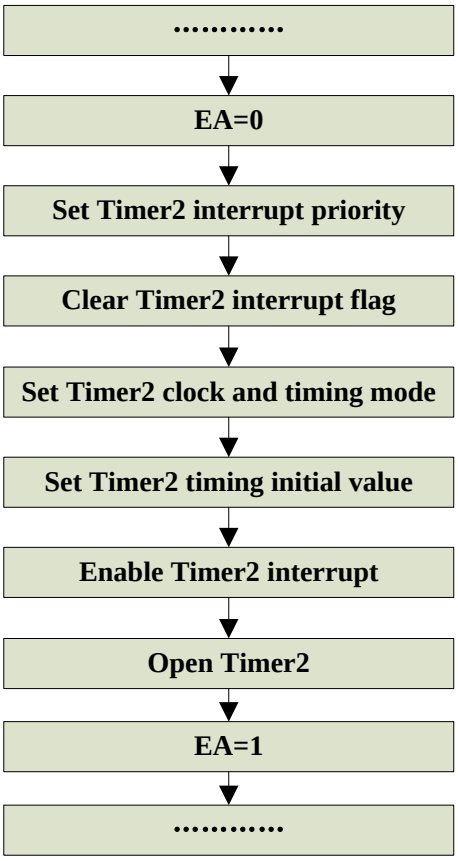
Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2 interrupt priority. 0: low priority; 1: high priority

PD_ANA (FEH) Module switch control register

Bit number	7~4	3	2	1	0
Symbol	-	PD_OSC_32K	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	1	1	1

Bit number	Bit symbol	Description
3	PD_OSC_32K	LIRC control register 1: off; 0: on, default on
2	PD_XTAL_32K	RTC crystal oscillator circuit (32768Hz) control register. 1: close; 0: open; default close.

8.2.3. Timer2 Configure Process



Timer2 configure process table

In the configuration process:

1. First configure the timing set value register TIMER2_SET_H/TIMER2_SET_L and step configuration TIMER2_CNT_MOD;
2. Then automatically reload the enable register TIMER2_RLD according to the configuration, set to 1 if automatic loop count is required, otherwise configure 0;
3. Final configuration timing enable register TIMER2_EN, enable timing configuration TIMER2_EN=1;
4. Stop timing: TIMER2_EN=0.

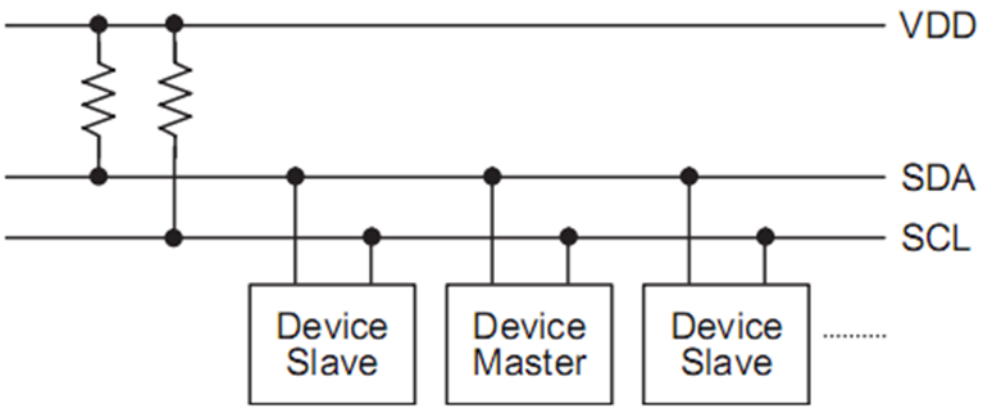
Notes:

1. **TIMER2_EN=0x1 to be placed at the end of all configurations;**
2. **During the TIMER2 timing, it is forbidden to change the configuration of Timer2. To modify, you need to stop timing first;**
3. **For precise timing, in the auto-reload mode, it is not allowed to configure three registers of TIMER2 in interrupt processing.**

9. IIC

The BF7412AMXX-XJLX supports standard and fast IIC communication, and has the following characteristics:

- Two serial interfaces: serial data line SDA and serial clock line SCL;
- Meet philips's standard communication protocol;
- Transmission rate: 100Kbps, 400Kbps;
- Support for 7-bit address addressing;
- Has the function of extending the clock low level;
- Wake-up core can be interrupted by IIC in low_power mode;
- Detect write conflicts and cache BUF overflow exceptions;
- Support digital filter function and analog filter function of IIC port.



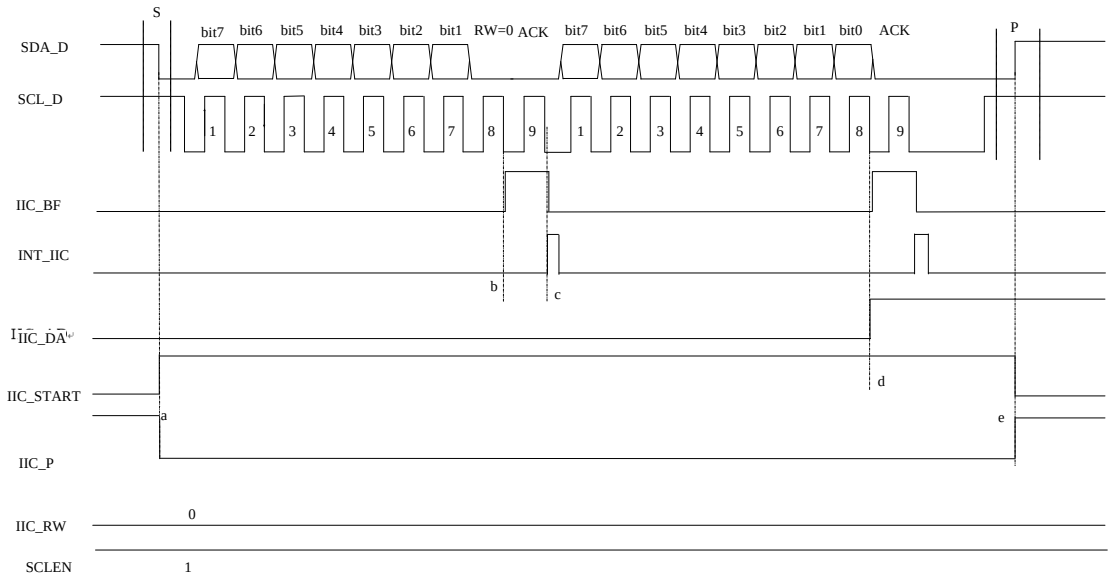
IIC host-slave

The host and slave from the SCL (serial clock) line, SDA (serial data) wire connection, in the communication mode, the PA0/PA1/PD6 is open drain, SCL, SDA must be connected to the pull resistor(suggest 4.7k~10k). When the TS device has touch related actions, such as touch, slide, figure away, etc. The host can read the state of the slave through IIC communication.

9.1. Communication Timing

The BF7412AMXX-XJLX uses hardware slave. When the host reads/writes data, after the slave receives the address, if the address matches, an interrupt is generated and a valid response signal is sent. And an interrupt is generated after the host computer writes the eighth clock of the data, and the host will not generate an interrupt signal when sending the stop signal. IIC timing diagram as follows:

IIC host write timing diagram



IIC write not pull down clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled down during the host write operation. From this, you can see the changes of the IIC bus and some internal signal changes.

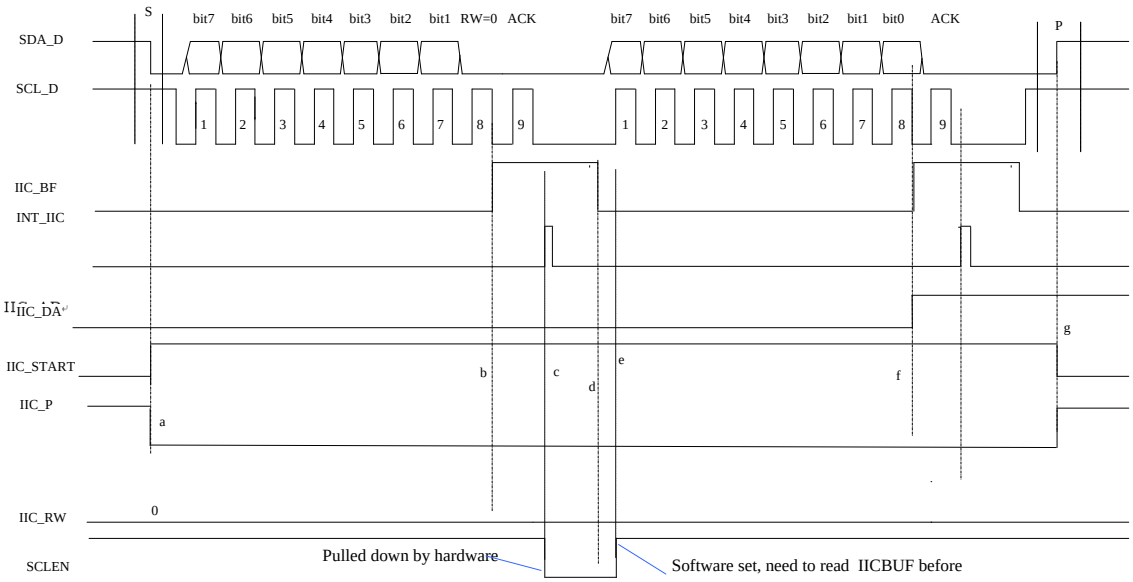
First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a in the figure.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b in the figure. An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c. The MCU executes interrupt subroutine device needs to read IICBUF. Even if this data is not useful, it needs to be operated.Reading the IICBUF operation will indirectly clear the START_BF. The host continues to send messages. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set. The currently received byte of the flag is data, and the stop signal has no effect on the IIC_STOP flag. That is, the stop signal IIC_STOP is detected, as shown by the dotted line d. And the IIC_AD flag will not be cleared. The interrupt is generated after the

falling edge of the ninth clock, and the interrupt subroutine requires the same operation. If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host write pull low timing diagram



IIC write low clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b.

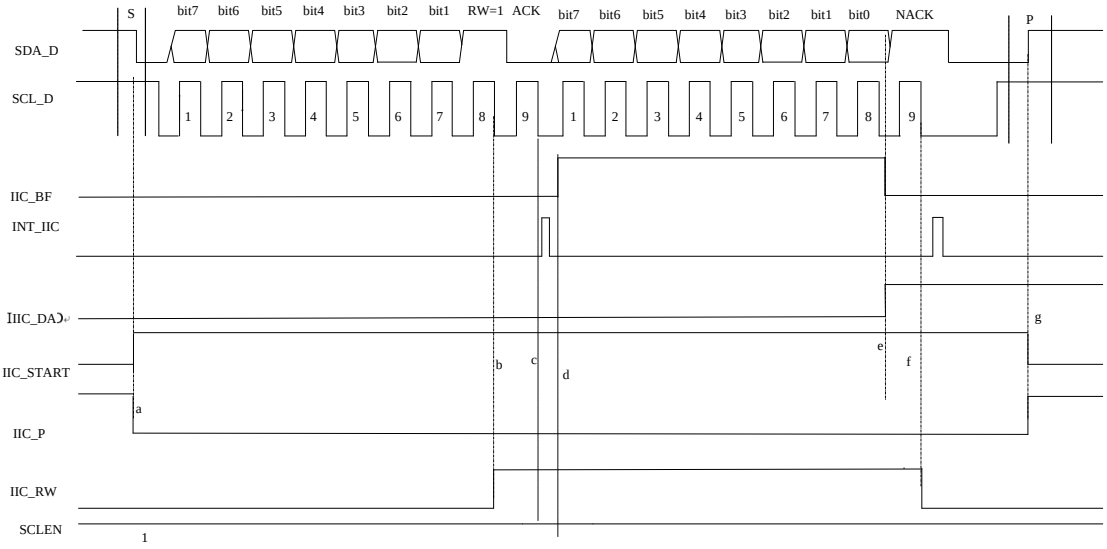
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c. SCLEN will be cleared by hardware. This process is used to process or read data from the slave. Even if this data is not useful, reading IICBUF will cause IIC_BUF to be cleared indirectly, as shown by the dotted line d. Software sets SCLEN to release the clock line.As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set. And the IIC_AD flag is also set. The currently received byte of the flag is data, as shown by the dotted line f, and the stop signal has no effect on the IIC_STOP flag. That is, the stop signal IIC_STOP is detected, and the IIC_AD flag will not be cleared; The interrupt is generated

after the falling edge of the ninth clock, and the interrupt subroutine requires the same operation. If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host read timing diagram



IIC host does not pull low clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled when the host reads.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address bytes and write flag bit, IIC_RW = 1, indicates that the host reads the slave. The slave automatically compares with its own address after receiving the address byte.Status bit IIC_RW set. As shown by the dotted line b. Set IIC_RW after the falling edge of the ninth clock if the address matches.

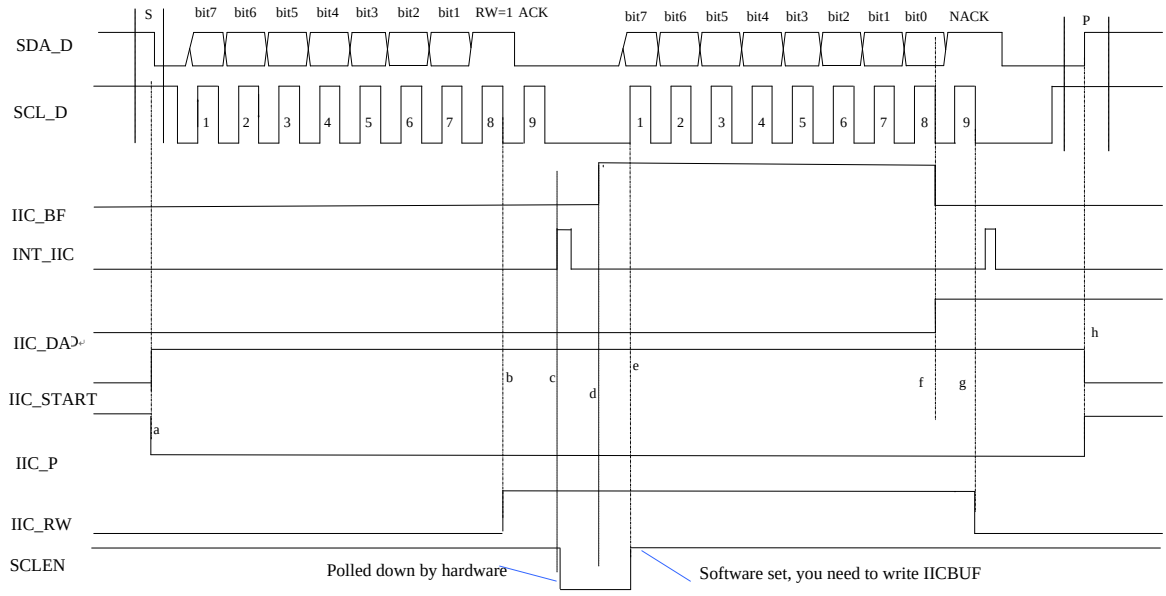
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. Ballast the data in IICBUFFER to IICBUF, IIC is set to clear, as shown by the dotted line d, and the highest bit is sent to the bus. After the eighth clock, one byte of data is sent, IIC_BF is set to clear; At the same time, the address data flag will also be set, indicating the currently transmitted byte data.

As shown by the dotted line e. An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate. If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. This should be noted in the application. When the NACK is detected, the read/write flag IIC_RW is

cleared by hardware. As shown by the dotted line f. If the host sends a NACK, the slave SCLEN will not be automatically pulled low.

Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line g. The bus enters the idle state.

IIC host read pull low timing diagram



IIC host read pull low clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled when the host reads.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address byte after the IIC_START signal. IIC_RW = 1, indicates that the host reads the slave. Status bit IIC_RW set. As shown by the dotted line b. Will not be set if the addresses do not match.

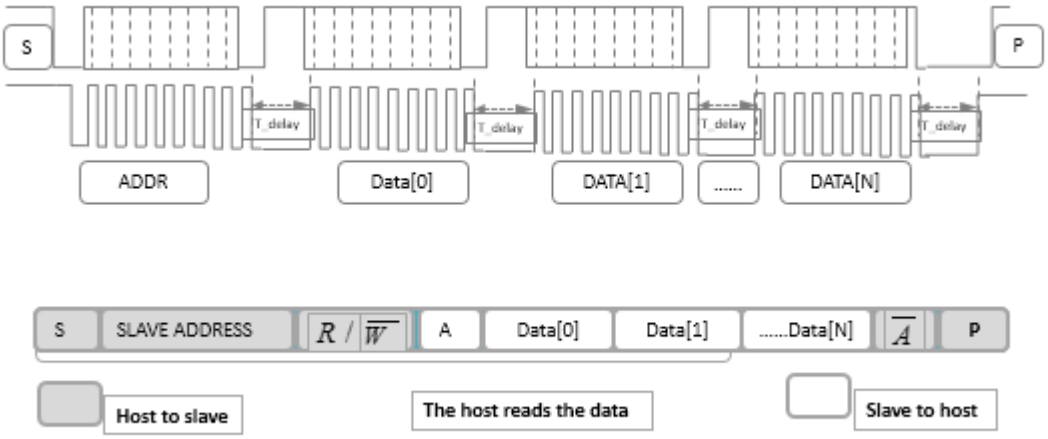
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. SCLEN will also be automatically pulled low by the hardware after the falling edge of the ninth clock. This period is used to process or prepare data from the slave, then write the prepared data to IICBUF, set SCLEN in software, and release the clock line. As shown by the dotted line d. In writing the data to the IIC, the IIC will be set, indicating that the IIC is full at this time. As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock and read the slave data. After the falling edge of the 8th clock, one byte of data has been sent and IIC_BF cleared; At the same time, the address data flag will also be set, indicating the currently transmitted byte data. As shown by the dotted line f.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to continue to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate; If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. When the NACK is detected, the read/write flag IIC_RW is cleared by hardware. As shown by the dotted line g.

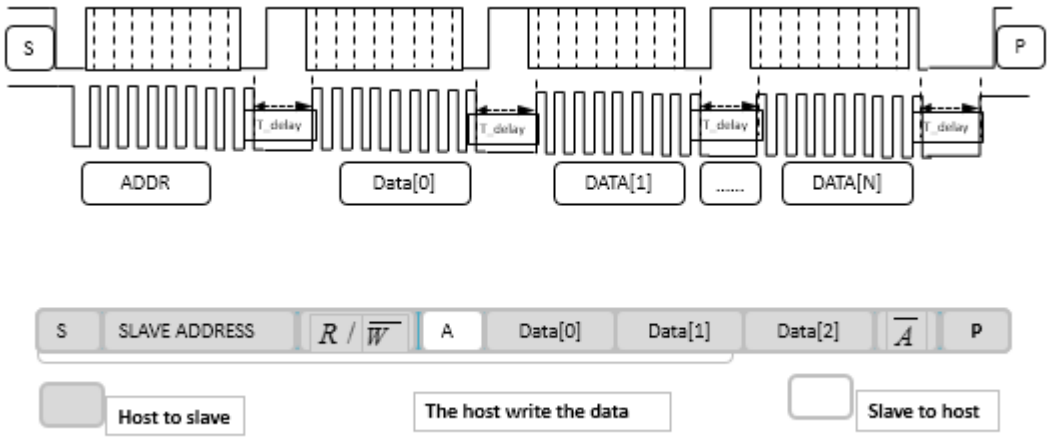
Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line h. The bus enters the idle state.

IIC host read data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us.

IIC host write data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us .

At the eighth clock slave send ack, IIC interrupt occurs at the ninth clock fulling edge.It is

recommended that the host delay 60us~300us when the ninth clock fulling edge is sent. Reserve the slave IIC interrupt service data preparation time, and then send the clock signal.

Note: When IIC communication>=100K, it is recommended that the system clock is 6MHz.

9.2. IIC Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description function**
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE8	IICSTAT	RO/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	PERIPH_IO_SEL	RW	x100_0000b	IIC /INT function control register
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1

IIC registers list

9.3. IIC Register Detailed Description

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

Bit number	Bit symbol	Description
7~1	IICADD[7:1]	IIC address register

IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit receive data buffer

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	–	–	IIC_RST	RD_SCL_EN
R/W	–	–	R/W	R/W
Reset value	–	–	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation 0: IIC module works properly
4	RD_SCL_EN	Host read pull low clock line control bit. 1: enable the host to read and pull the low clock line function; 0: disable the host to read and pull the low clock line function.
3	WR_SCL_EN	Host write pull low clock line control bit. 1: enable the host to write and pull the low clock line function; 0: disable the host to write and pull the low clock line function.
2	SCLEN	IIC clock enable bit 1: clock work properly 0: pull down the clock line.
1	SR	IIC conversion rate control bit 1: Conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC normal work; 0: IIC not work

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description

3	EX3	IIC interrupt enable 1: interrupt enable; 0: interrupt disable

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: start bit detected; 0: no start bit detected
6	IIC_STOP	Stop signal flag 1: stop status detected; 0: no stop status detected
5	IIC_RW	Read and write flag. Record the read/write information obtained from the address byte after the last address match. 1: read; 0: write.
4	IIC_AD	Address data flag 1: The most recently received or sent byte is data; 0: The most recently received or sent byte is address
3	IIC_BF	IICBUF full flag. Received in IIC bus mode: 1: received successfully, buffer is full; 0: received successfully, buffer is empty. Send in IIC bus mode 1: data transmission is in progress (does not include the acknowledge bit and the stop bit), buffer is full; 0: data transmission has been completed (does not include the acknowledge bit and the stop bit), buffer is empty.
2	IIC_ACK	Answer flag 1: invalid response signal; 0: effective response signal.
1	IIC_WCOL	Write conflict flag. 1: when the IIC is transmitting the current data, the new data

		is attempted to be written to the transmit buffer; new data cannot be written to the buffer. 0: no write conflict
0	IIC_RECOV	Receive overflow flag bit 1: When the previous data received by the IIC has not been taken, new data is received, the new data cannot be received by the buffer. 0: no receive overflow.

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUFFER	IIC transmit receive data buffer register. RD_SCL_EN=0, when the host reads the data, the data in the IICBUFFER is send to the slave transmit buffer after 2 clocks after the interrupt is generated, the data sent as a salve. Therefore, the previously prepared IICBUFFER interrupt data is generated before the interruption.

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	IE3	IIC interrupt flag 1: There is a IIC interrupt flag; 0: No IIC interrupt flag

PERIPH_IO_SEL (F2H) IIC /INT function control register

Bit number	7	6	5	4	3
Symbol	-	IIC_AFIL_SEL	IIC_DFIL_SEL	IIC_IO_SEL	
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	1	0	0	0
Bit number	2	1	0	/	
Symbol	INT2_IO_SEL	INT1_IO_SEL	INT0_IO_SEL	/	
R/W	R/W	R/W	R/W		

Reset value	0	0	0	

Bit number	Bit symbol	Description
6	IIC_AFIL_SEL	IIC port analog filter selection enable 1: select analog filter function; 0: do not select analog filter function.
5	IIC_DFIL_SEL	IIC port digital filter selection enable. 1: select digital filter function; 0: do not select digital filter function.
4~3	IIC_IO_SEL	IIC select enable 0: PA0/PA1 select IIC function; 1: PB5/PC0 select IIC function; 2: PA1/PD6 select IIC function (When PB5/PC0 is used as IIC port, there is no SR control function, automatic logic control becomes open-drain output, when PB5/PC0 is used as GPIO, there is no open-drain output function)

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
3	IPL1.3	IIC interrupt priority. 0: low priority; 1: high priority

9.4. IICSTAT Register

The IIC status register is used to reflect the status in the communication process and can be inquired by the user. Bit0 and Bit1 are readable and writable, and the other bits are read-only.

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: start bit detected; 0: no start bit detected
6	IIC_STOP	Stop signal flag 1: stop status detected; 0: no stop status detected
5	IIC_RW	Read and write flag. Record the read/write information obtained from the address byte after the last address match. 1: read; 0: write.
4	IIC_AD	Address data flag 1: The most recently received or sent byte is data; 0: The most recently received or sent byte is address
3	IIC_BF	IICBUF full flag. Received in IIC bus mode: 1: received successfully, buffer is full; 0: received successfully, buffer is empty. Send in IIC bus mode 1: data transmission is in progress (does not include the acknowledge bit and the stop bit), buffer is full; 0: data transmission has been completed (does not include the acknowledge bit and the stop bit), buffer is empty.
2	IIC_ACK	Answer flag 1: invalid response signal; 0: effective response signal.

1	IIC_WCOL	Write conflict flag. 1: when the IIC is transmitting the current data, the new data is attempted to be written to the transmit buffer; new data cannot be written to the buffer. 0: no write conflict
0	IIC_RECOV	Receive overflow flag bit 1: When the previous data received by the IIC has not been taken, new data is received, the new data cannot be received by the buffer. 0: no receive overflow.

IIC_START: Start signal status bit, IIC_START is set when the start signal is detected, Indicating that the bus is busy.

IIC_STOP: Stop signal status bit, IIC_START is set when the start signal is detected, indicating that the bus is idle. When the start signal is detected, the hardware is cleared, indicating that communication begins.

IIC_AD: Address data flag. It indicates whether the byte currently received or sent is an address or data. IIC_AD =0, flag is currently received or sent byte is the address; IIC_AD = 1 flag is currently received or sent byte is the data; Start signal, stop signal, non-response signal have no effect on this status bit. This status bit change occurs on the falling edge of the eighth clock.

IIC_RW: Read and write flag. The flag bit is recorded the read and write information bits obtained from the address is matched. IIC_RW = 1 means the host reads the slave. RW = 0 means the host writes the slave. Start signal, stop signal, non-answer signal (NACK) is cleared IIC_RW. This status bit change occurs on the falling edge of the eighth clock.

IIC_BF: BUFFER full flag. It indicates that the transceiver buffer is currently full or empty. IIC_BF=0 indicates that the buffer does not receive data and the buffer is empty; IIC_BF=1 indicates that the buffer receive data and the buffer is full. This status bit can only be set and cleared indirectly, not directly.

Address matching and IIC_RW=0, IIC_BF will be set after the falling edge of the eighth clock, indicating that the IICBUF has received the data. The IICBUF should be read during the execution of the interrupt routine, and the read IICBUF will indirectly clear the BF flag. If the host does not read IICBUF and the host continues to send data, a receive overflow will occur. Although the slave still receives the host to send data and is ballasted to the IICBUF.

IIC_RW=1 indicates the operation of the master to read the slave, the slave operation needs to write data to the IICBUF, and the slave writes IICBUF operation to set the IICBUF. The software then sets SCLEN to release the clock line; The host The host sends the synchronous clock. After the 8th clock is passed, the IICBUF is cleared by hardware after the data in the IICBUF is sent out.

IIC_ACK: Answer flag. Regardless of whether the host is a read or write operation, the slave samples the data line from the rising edge of the ninth clock and records the response information. The acknowledge bits are divided into a valid acknowledgment ACK and a non-valid acknowledgement bit NACK. That is to say, the rising edge of the ninth clock samples the data to 0,

indicating that the ACK is valid, and the IIC_ACK is cleared. If data 1 is sampled, NACK is set, indicating non-response. After the non-acknowledgment signal, the host will send a stop signal to announce the end of the communication. The start signal will clear this status bit.

IIC_WCOL: Write conflict flag. IICBUF only when IIC_RW=1, RD_SCL_EN＝1 and SCLEN＝0 can be written by the CPU. Any other attempt to write to IICBUF is forbidden. If the above conditions are not met, the write IICBUF operation occurs. Then the data will not be written to IICBUF, and the conflict flag IIC_WCOL will be set. This flag needs to be cleared by software.

IIC_RECOV: Receive overflow flag.In the case of IICBUF full, that is, in the case of data in the IICBUF. If IIC received new data, it will receive overflow and IIC RECOV will set.At the same time, the data in the IICBUF will not be updated, and the newly received data will be lost. This status bit also requires software to clear, otherwise it will affect the subsequent communication. This kind of situation will only appear in IICRW=0. BF=1, and the CPU will appear when it does not read IICBUF.

9.5. IICCON Register

The IICCON register is used to control the communication operation.

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	–	–	IIC_RST	RD_SCL_EN
R/W	–	–	R/W	R/W
Reset value	–	–	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation 0: IIC module works properly
4	RD_SCL_EN	Host read pull low clock line control bit. 1: enable the host to read and pull the low clock line function; 0: disable the host to read and pull the low clock line function.
3	WR_SCL_EN	Host write pull low clock line control bit. 1: enable the host to write and pull the low clock line function; 0: disable the host to write and pull the low clock line function.
2	SCLEN	IIC clock enable bit 1: clock work properly 0: pull down the clock line.
1	SR	IIC conversion rate control bit 1: Conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC normal work; 0: IIC not work

The role is describle in detail below:

IICEN is module enable signal, when IICEN=1, the circuit works.

SR is the conversion rate control bit, SR=1 conversion ratecontrol off, port adapted to 100Kbps communication.

SCLEN is clock enable control bit, although the slave cannot generate the communication clock, the slave can extend the low time of the clock according to the protocol. SCLEN=0, clock line is locked at low level; SCLEN=1, release clock line. The premise of extending the low level of the clock is IICEN=1, otherwise the internal circuit will not have any effect on the IIC bus. SCLEN is often used to extend low time and make the host enter the wait state, so that the slave has enough time to process the data.

WR_SCL_EN is write low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

IIC_RW=0, according to the communication rate of the host and the time of processing the interrupt, it is determinded whether to lower the clock line, that is, configure the WR_SCL_EN bit.

When the CPU can process the interrupt and exit the interrupt within 8 IIC clocks. WR_SCL_EN=0 disable pull down the clock clock line function. At this time, the hardware will not automatically pull down the clock line when the interrupt arrives. When the CPU cannot process the interrupt and exit in the 8 IIC clocks, WR_SCL_EN=1 enables the clock line to be pulled down. At this point, the hardware automatically pulls down the clock line when the interrupt arrives, forcing the host to enter the wait state. When the data written to the IIC is read by the CPU, the software sets SCLEN.

RD_SCL_EN is read low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

RD_SCL_EN=1, when the slave receives the address byte or sends one byte and the host sends, SCLEN wll be automatically pulled low by hardware, forcing the host to the enter the wait state. The release the IIC clock from the slave, the following two operations arerequired: first write the data to be sent to the IIC, set the software in IICBUF in SCLEN. The purpose of this design is to ensure that the data to be sent has been written in the IICBUF before the SCL is pulled high.

RD_SCL_EN=0, when the slave receives the address byte or sends one byte and the host sends an ACK, the slave immediately polls the data prepared in the IICBUFFER register to the transmit buffer register and then to the data line. Therefore, in order to ensure that data transmitted each time is correct, IICBUFFER prepares the next data to be sent in the interrupt service routine. The data received by the host is the last interrupted data, and the first time the data is received is ready for initialization.

Note: When you need to pull down the clock line, that is, WR_SCL_EN/RD_SCL_EN=1. Software should turn off the clock line until the last Byte data is sent and received. That is, WR_SCL_EN/RD_SCL_EN=0, the software should turn on the write low pull clock line before sending and receiving the last Byte data. This kind of operation can be self-regulated according to whether the host is software or hardware.

IIC_RST is IIC module control enable bit, enable the IIC module reset function for 1 and disable the IIC module reset function when 0. Pay attention to configuration 1 reset IIC module all DFF triggers. The reset terminal of IIC_RST is global reset, and the other reset terminal are iic_rst_n. All iic_rst writes 0 first, then operate other register configurations.

9.6. IICBUF Register

The IICBUF register is used to control the communication operation.

IICBUF (E4H) IIC transmit and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

The specific application process is as follows:

In the send state, after the data is ballasted into the IICBUF, under the synchronous clock of the host. The data is sequentially shifted and sent out, the high position is in front. After 8 clocks, one byte is sent.

In the receive state, after the host's 8 clocks have passed, the data is written to the BUF. After the 9th clock, an interrupt is generated, telling the CPU to read the data in the IICBUF.

Writing data to IICBUF is conditional, when RD_SCL_EN=1, only IIC_RW=1, and SCLEN=0 can write data into IICBUF; Otherwise, the operation of writing IICBUF is prohibited. That is to say, if the condition is not satisfied, the operation of writing IICBUF cannot be successful, and the data cannot be written. IICBUF data will not change, but will also cause write confilicts.

For example: IICBUF already has been 55h. In case the condition of writing IICBUF is not satisfied, we want to write data 00h into IICBUF. The result is that the data in IICBUF is still 55h, and the write conflict flag IIC_WCOL is set to tell the user that the operation is abnormal.

When RD_SCL_EN=0, the data to be the slave is the value of the ballast IICBUFFER register when the interrupt signal is generated.

9.7. IICBUFFER Register

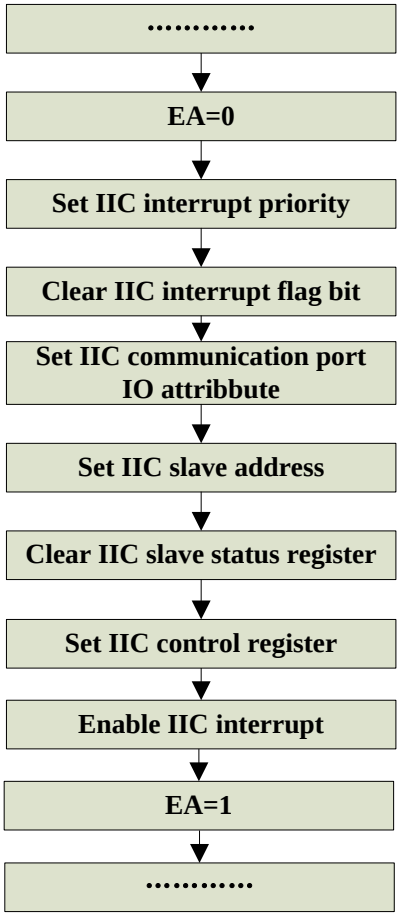
IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

The specific application process is as follows:

When RD_SCL_EN=0, and the host reads the data, the data in the IICBUFFER is sent to the slave transmit buffer register after the two clks after the interrupt is generated, and the data is sent as slave. Therefore, the data in the IICBUFFER should be prepared before the interrupt is generated. Generally, it is ready in the service routine. Device address generation interrupts send data to prepare for initialization.

9.7. IIC Configure Process



IIC configure process

Notes: IIC bus pull-up resistor 4.7K~10K, ground filter capacitor 10pF~ 100pF close to the lead chip.

10. UART

There are 2 UART modules in the BF7412AMXX-XJLX series. UART0 supports 6 IO port mapping, and UART1 supports 2 channels. Only one set of mapping can be mapped at the same time. UART module interface characteristics:

- Support full-duplex, half-duplex serial
- Independent dual buffer receiver and single buffer transmitter
- Programmed baud rate (10bit analog-to digital divider)
- Interrupt-driven or polling operation:
  - send completed
  - receiving full
  - receive overflow, parity error, frame error
- Supports hardware parity production and check
- Programmable 8bit or 9bit character length
- STOP bit 1 or 2 can be selected
- Supports multiprocessor mode
- Support TXD/RXD pin position swap
- Support TXD/RXD independent enable

10.1. UART Function Description

10.1.1. Baud Rate Generation

Baud rate generation modules: Baud_Mod= {UART0/1_BDH[1:0], UART0/1_BDL}.

Baud rate calculation formula: Baud_Mod=0, does not generate baud rate clock. When Baud_Mod=1~1023, UART0 baud rate = BUSCLK/(16x Baud_Mod).

The BUSCLK uses the divided clock of the system clock source, fixed to 24M. Each time the baud rate register is configured, the internal counter is cleared and the baud rate signal is regenerated. Communication requires the transmitter and receiver to use the same baud rate. Baud rate deviation range allowed by communication: 8/(11*16)=4.5%.

10.1.2. Transmitter Function

Send data flow: Trammitted by writing UART0/1_BUF data, sending stop bit after sending stop bit. Software clear interrupt flag and waits for the next write. The transmitter output pin (TXD) idle state defaults to a logic high state. The entire transmission process must be performed when the module is enabled.

By writing data to the data register (UART0/1_BUF), save the data directly to the send data buffer and start the send process. The data buffer is locked during the subsequent complete transmission.The configuration write data register UART0/1_BUF and T8 is invalid. After the stop bit is sent, writing to UART0/1_BUF again will restart the new transmission.

The serial component of the serial transmitter has a length of 10/11/12 (depending on the setting in the data_mode control bit) transmit shift register. If data_mode=0, select normal 8bit data mode. In the 8bit data mode, there is 1 start bit in the shift register, 8 data bits and 1/2 stop bits. Send and receive are small endian mode (LSB first).

10.1.3. Receiver Function

The receiver is enabled by setting the receive enable bit in UART0/1_CON1. The entire receiving process must be performed when the module is enabled.

Receiving data flow: receive data at any time with the reception enable enabled. After receiving the stop bit, set the middle segment and the software clears the interrupt flag.

Currently acceptly data will detect wit, detect receive overflow, frame error, parity error three errors. Software clearance mark required. It is recommended to read the status flag and read the data buf after receiving the receive interrupt. Finally, the received data status flags are cleared.

Data character is started by logic 0, 8 or 9 data bit (LSB send first) and stop bits (1bit) of logic 1. After receiving the stop bit to the shifter, if the receive data shift register is not full (RI0/1=0), data characters are transferred to the receive data register, setting the receive data register full (RI0/1=1) status flag. If the rx_full_if of the receive data register is already set at this time, set the overflow (UART0/1_RO) status flag, the new data will be lost. Because the receiver is double

buffered, after setting rx_full_if, program has a full character time for reading before reading the data of the receive data buffer to avoid receiver overflow.

When the program detects that the receive data register is full (RI0/1=1), it acquires data from the receive data register by reading UART0/1_BUF.

10.1.4. Receiver Sampling Method

The receiver uses with a 16x baud rate clock for sampling. The receiver searches for falling edge on the RXD serial data input pin by extracting the logic level samples at 16x baud rate.The falling edge is defined as the logic 0 level after 3 consecutive logic 1 samples. The 16x baud rate clock is used to divide the bit time into 16 segements, labeled RT1 and RT16 respectively.

The receiver then samples at each bit time of RT8, RT9 and RT10, including the start and stop bits to determine the logic level of the bit. The logic level is the logic level of most samples advanced during the bit time period. When the falling edge is located, the logic level is 0 to ensure that this is the true starting bit, not the noise. If at least two of the three samples are 0, the receiver assumes that it is synchronized with the receiver character. Start shifting to receive the following data, if the above conditions are not met, exit the state machine and return to the waiting for falling edge state.

The falling edge detection logic constantly looks for the falling edge. If an edge is detected, the sample clock resynchronizes the bit time. This improves the reliability of the receiver when noise or mismatch in baud rate occurs.

10.1.5. Multiprocessor Mode

Multiprocessor mode, only works in 9-bit mode, when the received UART0/1_R8 bit=1, the receive interrupt is set, otherwise it is not set. The role of this mechanism is to eliminate the software overhead of handing unimportant information for diffrernt receivers.

In this application system, all receivers estimate the address character (ninth bit=1) of each message. Once it is determined that the information is intended for different receivers, subsequent data characters (ninth bit=0) are not received.

Configuration process: configuring receive enable, configuring multiprocessor mode, received address data (ninth bit=1), receive and generate an interrupt. The application confirms that the addresses match, and the match configures to turn off the multiprocessor mode. All subsequent data (ninth bit=0) can be received and interrupted until the next time the address data is received, the address does not match, then the multiprocessor mode is turned on. Then all subsequent data is not received until the next address data, and then cyclically applied.

10.2. UART Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xB1	UART_IO_SEL	RW	xxxx_0000b	UART select enable register
0xBD	UART0_BDL	RW	0000_0000b	UART0 Baudrate control registe
0xBE	UART0_CON1	RW	0000_0000b	UART0 control register 1
0xBF	UART0_CON2	RW	0000_1100b	UART0 control register 2
0xC0	UART0_STATE	RO/RW	x000_0000b	UART0 status flag register
0xC1	UART0_BUF	RW	1111_1111b	UART0 data register
0xC5	UART1_BDL	RW	0000_0000b	UART1 baud rate control register
0xC6	UART1_CON1	RW	0000_0000b	UART1 control register 1
0xC7	UART1_CON2	RW	xxx0_1100b	UART1 control register 2
0xC8	UART1_STATE	RO/RW	x000_0000b	UART1 status flag register
0xC9	UART1_BUF	RW	1111_1111b	UART1 data register
0xE1	IRCON2	RW	xxxx_x000b	Interrupt flag register 2
0xE7	IEN2	RW	xxxx_x000b	Interrupt enable register 2
0xF4	IPL2	RW	xxxx_x000b	Interrupt priority register 2

UART registers list

10.3. UART Register Detailed Description

UART_IO_SEL (B1H) UART select enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	UART1_IO_SEL	UART0_IO_SEL		
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3	UART1_IO_SEL	UART1 port selection enable 0: PB1/2 (RXD1_A/TXD1_A) port select UART1 port function 1: PB6/7 (RXD1_B/TXD1_B) port select UART1 port function
2~0	UART0_IO_SEL	UART0 port selection enable 000: PA0/1 (RXD0_A/TXD0_A) port select UART0 port function 001: PB3/4 (RXD0_B/TXD0_B) port select UART0 port function 010: PD4/5 (RXD0_C/TXD0_C) port select UART0 port function 011: PC0/1 (RXD0_D/TXD0_D) port select UART0 port function 100: PD6/PA1 (RXD0_E/TXD0_E) port select UART0 port function

		101: PD7/PA0 (RXD0_F/TXD0_F) port select UART0 port function

UART0_BDL (BDH) UART0 Baudrate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Baud rate control register. Baud rate modules divisor register lower 8 bits, bandrate={UART0_BDH[1:0], UART0_BDL}, bandrate=0, does not generate baud rate clock. bandrate=1~1023, bandrate = BUSCLK/(16xbandrate)

UART0_CON1 (BEH) UART0 control register 1

Bit number	7	6	5	4
Symbol	UART0_ ENABLE	TRANS_ ENABLE	RECEIVE_ ENABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART0_ENABLE	Module enable. 1: module enable; 0: module off.
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable. 1: receiver open; 0: receiver off.
4	MULTI_MODE	Multiprocessor communication mode. 1: mode enable; 0: mode disable.
3	STOP_MODE	Stop bit width selection.

		1: 2 bit; 0: 1 bit.
2	DATA_MODE	Data mode select. 1: 9bit mode; 0: 8bit mode.
1	PARITY_EN	Parity enable. 1: parity enable; 0: parity disable.
0	PARITY_SEL	Parity select. 1: odd parity; 0: even parity.

UART0_CON2 (BFH) UART0 control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	PAD_CHANGE	TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	-	R/W	R/W	R/W	R/W	
Reset value	-	-	-	0	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	Txd/rxd pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Send interrupt enable. 1: interrupt enable; 0: interrupt disable (used in polling mode)
2	RX_FULL_IE	Received interrupt enable 1: interrupt enable; 0: interrupt disable (used in polling mode)
1~0	UART0_BDH	Baud rate modulus divisor register high 2bit.

UART0_STATE (C0H) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	Receiver’s ninth data, read only.

5	UART0_T8	Transmitter's ninth data, read only when parity is enabled.
4	TI0	Send interrupt flag. 1: send buffer is empty; 0: send buffer is full, software write 0 clear 0, write 1 invalid.
3	RI0	Receive interrupt flag. 1: receive buffer is full; 0: receive buffer is empty, software write 0 clear 0, write 1 invalid.
2	UART0_RO	Receive overflow flag; 1: receive overflow (lost new data); 0: no overflow, software write 0 clear 0, write 1 invalid.
1	UART0_F	Framing error flag. 1: framing error flag; 0: no framing error flag, software write 0 clear 0, write 1 invalid.
0	UART0_P	Parity error flag. 1: receiver parity error; 0: parity is correct, software write 0 clear 0, write 1 invalid.

UART0_BUF (C1H) UART0 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Data register Read returns read-only receive data buffer contents, write into write-only send data buffer.

UART1_BDL(C5H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	-	Baud rate control register The lower 8 bits of the baud rate modulus divisor register, Baud_Mod={UART1_BDH[1:0], UART1_BDL},

		When Baud_Mod=0, the baud rate clock is not generated, when Baud_Mod=1~1023, the baud rate = BUSCLK/(16xBaud_Mod)

UART1_C2(C6H) UART1 control register 3

Bit number	7	6	5	4
Symbol	UART1_ ENABLE	TRANS_ ENABLE	RECEIVE_E NABLE	MULTI_ MODE
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART1_ENABLE	Module enable 1: module enable; 0: module close
6	TRANS_ENABLE	Transmitter enable 1: transmitter is on; 0: transmitter is off
5	RECEIVE_ENABLE	Receiver enable 1: receiver is on; 0: receiver is off
4	MULTI_MODE	Multiprocessor communication mode 1: mode enable; 0: mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: parity check is enabled; 0: parity check is disabled
0	WAKE_SEL	Parity selection 1: odd parity; 0: even parity

UART1_CON2(C7H) UART1 control register 2

Bit number	7	6	5	4
Symbol	-	-	-	PAD_CHANGE
R/W	-	-	-	R/W
Reset value	-	-	-	0
Bit number	3	2	1	0
Symbol	TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	

R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	0

Bit number	Bit symbol	Description
4	PAD_CHANGE	Txd/rxd pin interchange 1: pin interchange; 0: the pins are not interchangeable
3	TX_EMPTY_IE	Transmit interrupt enable 1: interrupt enable; 0: interrupt disabled (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: interrupt enable; 0: interrupt disabled (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register high 2 bits

UART1_STATE (C8H) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	UART1_R8	UART1_T8	TI1
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W

Bit number	Bit symbol	Description
6	UART1_R8	The 9th data of the receiver, read only
5	UART1_T8	The 9th data of the transmitter, read only during parity check
4	TI1	Send buffer empty interrupt flag 1: The sending buffer is empty; 0: Send buffer is full, software write 0 to clear
3	RI1	Receive interrupt flag 1: The receive buffer is full; 0: Receive buffer is empty, software write 0 to clear
2	UART1_RO	Receive overflow flag 1: Receive overflow (new data is lost); 0: No overflow, software writes 0 to clear
1	UART1_F	Frame error flag 1: A frame error is detected; 0: No frame error is detected, software writes 0 to clear
0	UART1_P	Parity error flag

		1: Receiver parity error; 0: Parity check is correct, software writes 0 to clear

UART1_BUF (C9H) UART1 data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	-	Read returns the contents of the read-only receive data buffer, writes to the write-only send data buffer.

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IE10	IE9	IE8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2	IE10	UART1 interrupt flag 1: There is a UART1 interrupt flag; 0: No UART1 interrupt flag
1	IE9	UART0 interrupt flag 1: There is a UART0 interrupt flag; 0: No UART0 interrupt flag

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	EX10	EX9	EX8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

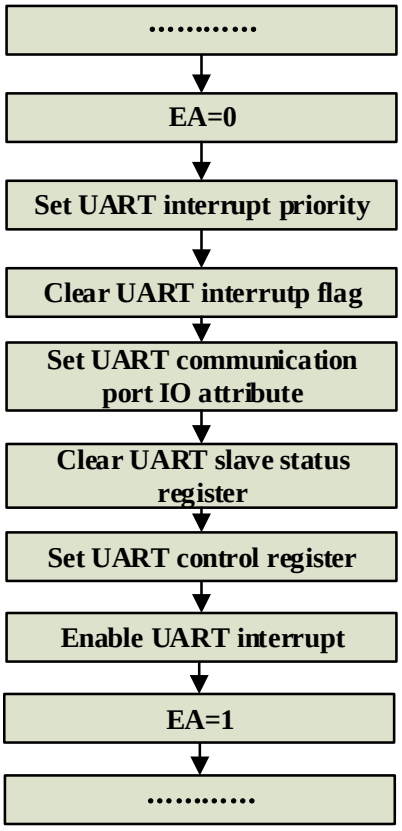
Bit number	Bit symbol	Description
7~3	-	Reserved
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
7~3	--	Reserved
2	IPL2.2	UART1 interrupt priority. 0: low priority; 1: high priority
1	IPL2.1	UART0 interrupt priority. 0: low priority; 1: high priority

10.4. UART Configuration Process



UART initial configuration process

UART suggested application process:

1. Configuration module enable, receive enable, mode select: UART0_CON1;
2. Configure baudrate, open interrupt enable: UART0_BDL, UART0_CON2;

3. Write UART0_BF starts to send data, after detecting the transmission interrupt, clear the interrupt flag TI0;

4. Receive interrupt detected, first read status UART0_STATE. Then read R8 and UART0_BUF, finally clear the receive status flag (UART0_STAT[3:0] = B0000). One receiving process is completed, waiting for the next receiving interrupt;

5. If the configuration interrupt is not enabled, the program executes the UART0 function. Also read the status flag first, then read UART0_R8 and UART0_BUF, and finally clear the status flag.

6. Interrupt flag clear operation. In full-duplex operation, clear flag bit operation requires a vaild interrupt bit to be written 0, and other interrupt bits to be written as 1 (write 1 as invalid operation), otherwise it is easy to operate incorrectly. For example: when the send interrupt is vaild, you need tp write UART0_STATE = 0x0F; (configuration UART0_STATE[0:3] = 0x0F, UART0_R8 write is invalid, UART0_T8 needs to configure vaild transmit data when it is in 9 bit mode and does not have parity).

7. 8 bit mode: Parity enable is valid.

9 bit mode: When the parity bit is enabled, when the parity bit calculated by the ninth bit is not enable, the ninth bit is the UART0_T8 written in. Only send interrupts and receive interrupts.The error flag only marks the error detection of the current data, and only the corresponding bit writes 0 clear, do not jump out of error interrupt. The transmit interrupt is set after the stop bit is sent, and the software clears it. The receive interrupt is set after the stop bit is sent, and the software clears it.

Multiprocessor mode: Only works in 9 bit mode, received UART0_R8= 1, receive interrupt is set, otherwise it is not set. When using multiprocessor mode, configuring receive enable and multiprocessor mode. Receive address data (the ninth bit=1) and generate an interrupt, confirm that the address matches. Matching configures the multiprocessor mode to be turned off, and all subsequent data (the ninth bit = 0) can be interrupted by the received interrupt, until the next time data is received. If the address do not match, the multiprocessor mode is turned on, and all subsequent data is not received until the next address data.

Hardware response: Send data is opened by the value written to UART0_BUF. The interrupt flag is sent after the stop bit is sent. The software clears the interrupt flag and waits for the next write. The receive data receives data at any time when the receiving enable is effective. Set receive interrupt after receiving stop bit, software clear interrupt flag. The currently received data has a detection mechanism that can detect three errors of receive overflow, frame error, and parity error. Both require a software clear flag. It is recommended to read the status flag after the receive interrupt and clear the receive status flag UART0_STATE[3:0].

8. It is recommended to change the configuration of UART0_CON1[4:0] and the baud rate register when the module is enabled and closed, otherwise it may be disordered and cause the communication function to malfunction.

Note: The mapping synchronization output function is not supported.

11. PWM

11.1. PWM0 Function Description

PWM0 Function Description:

- The clock source is the fixed clock PLL_12M;
- Support up to 4 channels, each channel is individually enabled
- 16bit counter;
- Configurable counting period, adjustable duty cycle of each channel;
- PWM output waveform polarity can be configured;
- The duty cycle of channel 1/2/3 can be selected as the same configuration as channel 0 or the duty cycle configuration of your own channel;
- Each channel can independently select 2 IO port mapping

The PWM0 module supports 4 channels. Each channel can be individually controlled and enabled, sharing a 16-bit counter. The counting clock is 12MHz. The period of the PWM0 signal is determined by the value of the period configuration register (PWM0_MOD), the duty cycle is determined by the setting in the channel register (PWM0_CHn_CNT), the polarity of the PWM0 signal is determined by the setting in the PWM0_CH_CTRL control bit, 0% and 100% Space ratios are all possible.

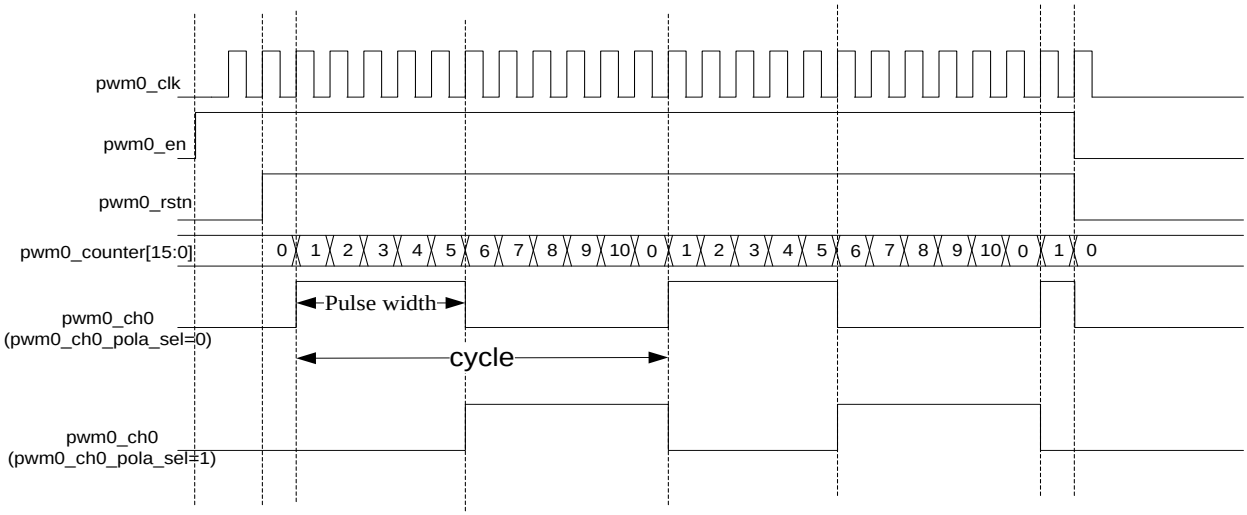
Pulse width = (PWM0_CHn_CNT)

Cycle = (PWM0_MOD+1)

Duty cycle = pulse width/period

PWM0 counter counts up from 0x0000, when PWM0_CHn_CNT is counted, the output is inverted. This time is the pulse width. Countine counting until the count overflows at PWM0_MOD+1. If PWM0_CH0_POLA_SEL=0, PWM0 signal enters high state when output is flipped. If PWM0_CH0_POLA_SEL=1, PWM0 signal enters high state when output is overflows.

When channel count register (PWM0_CHn_CNT) is set 0x0000, the duty cycle is 0. When channel count register (PWM0_CHn_CNT) is set to a value greater than the value set by the period configuration register (PWM0_MOD) to achieve a 100% duty cycle. The counter is automatically reloaded and will not stop by itself until the register PWM0 is enabled to stop and the counter is cleared.



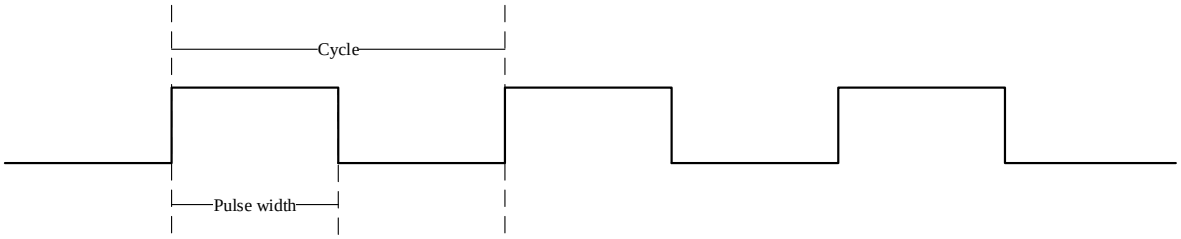
(PWM0_CH0_CNT=5, PWM0_MOD=10, duty_cycle=5/11)

11.2. PWM1/2 Function Description

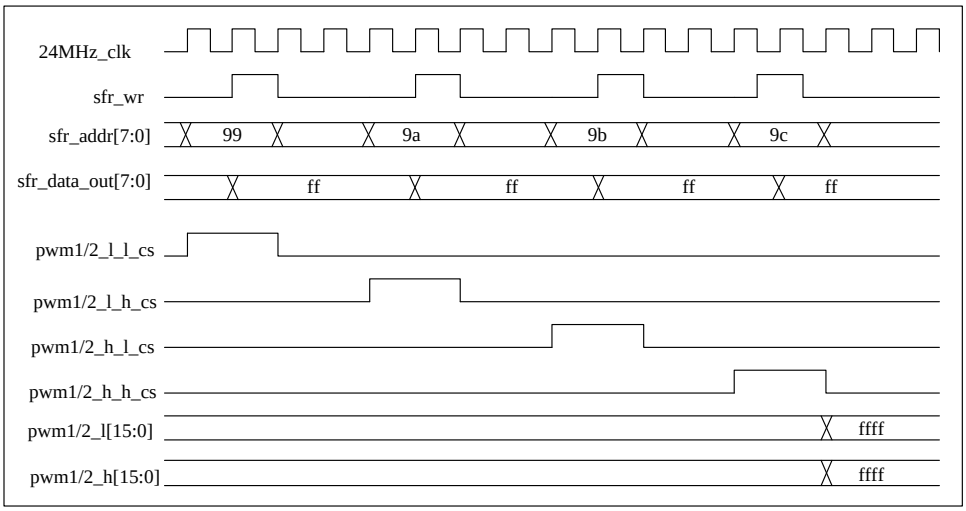
PWM1/2 features are as follows:

- The clock source is the fixed clock PLL_12M
- The high level control register and the low level control register are 16-bit registers
- Output cycle: $T_{PWM1/2\_data}$ = (PWM1/2_H + PWM1/2_L)* T_{12MHz} (μs)
- Output duty cycle: $D_{PWM1/2\_data}$ = PWM1/2_H/(PWM1/2_L + PWM1/2_H)
- Each channel can independently select 2 IO port mapping

Waveform diagram



The PWM1/2 pulse width modulation module's high and low time can be configured through the register, but the configuration of the register must be in the case of PWM1/2 enable effective (high effective), and the high level control register and low level control register must be configured in order from low to high, in order to ensure that the internal counter of the PWM1/2 module counts correctly and avoid generating wrong waveforms. These configuration values update the period and duty cycle after a complete period.



PWM1/2 timing diagram

11.3. PWM Related Registers

SFR register				
address	**name**	**R/W**	**Reset value**	**Description**
0x99	PWM1_L_L	RW	0000_0000b	PWM1 low level control register (low 8 bits)
0x9A	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8 bits)
0x9B	PWM1_H_L	RW	0000_0000b	PWM1 high level control register (low 8 bits)
0x9C	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8 bits)
0x9D	PWM2_L_L	RW	0000_0000b	PWM2 low level control register (low 8 bits)
0x9E	PWM2_L_H	RW	0000_0000b	PWM2 low level control register (high 8 bits)
0x9F	PWM2_H_L	RW	0000_0000b	PWM2 high level control register (low 8 bits)
0xA1	PWM2_H_H	RW	0000_0000b	PWM2 high level control register (high 8 bits)
0xA2	PWM_EN	RW	xx00_0000b	PWM control register
0xA3	PWM0_CH_CTRL	RW	0000_0000b	PWM0 control register
0xA4	PWM0_CH0_CNT_L	RW	0000_0000b	PWM0 channel 0 count value configuration register low 8 bits
0xA5	PWM0_CH0_CNT_H	RW	0000_0000b	PWM0 channel 0 count value configuration register high 8 bits
0xA6	PWM0_CH1_CNT_L	RW	0000_0000b	PWM0 channel 1 count value configuration register low 8 bits
0xA7	PWM0_CH1_CNT_H	RW	0000_0000b	PWM0 channel 1 count value configuration register high 8 bits
0xA9	PWM0_CH2_CNT_L	RW	0000_0000b	PWM0 channel 2 count value configuration register low 8 bits
0xAA	PWM0_CH2_CNT_H	RW	0000_0000b	PWM0 channel 2 count value configuration register high 8 bits
0xAB	PWM0_CH3_CNT_L	RW	0000_0000b	PWM0 channel 3 count value configuration register low 8 bits
0xAC	PWM0_CH3_CNT_H	RW	0000_0000b	PWM0 channel 3 count value configuration register high 8 bits
0xAD	PWM0_MOD_L	RW	0000_0000b	PWM0 cycle configuration register low 8 bits
0xAE	PWM0_MOD_H	RW	0000_0000b	PWM0 cycle configuration register high 8 bits
0xB2	PWM_IO_SEL	RW	xx00_0000b	PWM channel selection IO configuration register

PWM registers list

NOTE:

Channel 0: PWM0_A/A1; Channel 1: PWM0_B/B1;

Channel 2: PWM0_C/C1; Channel 3: PWM0_D/D1;

11.4. PWM Register Detailed Description

PWM1_L_L (99H) PWM1 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_L							
R/W	R/W							
Reset value	0							

PWM1_L_H (9AH) PWM1 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_L_H							
R/W	R/W							
Reset value	0							

PWM1_H_L (9BH) PWM1 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_L							
R/W	R/W							
Reset value	0							

PWM1_H_H (9CH) PWM1 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H							
R/W	R/W							
Reset value	0							

PWM2_L_L (9DH) PWM2 low level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_L							
R/W	R/W							
Reset value	0							

PWM2_L_H (9EH) PWM2 low level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_H							
R/W	R/W							
Reset value	0							

PWM2_H_L (9FH) PWM2 high level control register (low 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_L							
R/W	R/W							
Reset value	0							

PWM2_H_H (A1H) PWM2 high level control register (high 8 bits)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_H							
R/W	R/W							
Reset value	0							

PWM_EN (A2H) PWM control register

Bit number	7	6	5	4
Symbol	-	-	PWM0_CH3_CMOD	PWM0_CH2_CMOD
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH1_CMOD	PWM2_EN	PWM1_EN	PWM0_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	PWM0_CH3_CMOD	PWM0 channel 3 duty cycle mode select register 1: select channel 0 duty cycle 0: select its own channel duty cycle
4	PWM0_CH2_CMOD	PWM0 channel 2 duty cycle mode select register 1: select channel 0 duty cycle 0: select its own channel duty cycle
3	PWM0_CH1_CMOD	PWM0 channel 1 duty cycle mode select registe 1: select channel 0 duty cycle 0: select its own channel duty cycle
2~0	PWMn_EN (n=2,1,0)	PWMn module enable register 1: enable; 0: not enable

PWM0_CH_CTRL (A3H) PWM0 control register

Bit number	7	6	5	4
Symbol	PWM0_CH3_POLA_SEL	PWM0_CH2_POLA_SEL	PWM0_CH1_POLA_SEL	PWM0_CH0_POLA_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH3_EN	PWM0_CH2_EN	PWM0_CH1_EN	PWM0_CH0_EN
R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	PWM0_CH3_POLA_SEL	Channel 3 polarity selection ch3_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
6	PWM0_CH2_POLA_SEL	Channel 2 polarity selection ch2_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
5	PWM0_CH1_POLA_SEL	Channel 1 polarity selection ch1_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
4	PWM0_CH0_POLA_SEL	Channel 0 polarity selection ch0_pola_sel 1: count value overflow makes the output low 0: count value overflow makes the output high
3	PWM0_CH3_EN	Channel 3 enable ch3_en 1: enable 0: not enable
2	PWM0_CH2_EN	Channel 2 enable ch2_en 1: enable 0: not enable
1	PWM0_CH1_EN	Channel 1 enable ch1_en 1: enable 0: not enable
0	PWM0_CH0_EN	Channel 0 enable ch0_en 1: enable 0: not enable

PWM0_CH0_CNT_L (A4H) PWM0 channel 0 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH0_CNT_L	Channel 0 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH0_CNT_H (A5H) PWM0 channel 0 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH0_CNT_H							

R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	PWM0_CH0_CNT_H	Channel 0 count configuration register high 8 bits. Configure PWM output duty cycle.

PWM0_CH1_CNT_L (A6H) PWM0 channel 1 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH1_CNT_L	Channel 1 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH1_CNT_H (A7H) PWM0 channel 1 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH1_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH1_CNT_H	Channel 1 count configuration register high 8 bits. Configure PWM output duty cycle.

PWM0_CH2_CNT_L (A9H) PWM0 channel 2 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH2_CNT_L	Channel 2 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH2_CNT_H (AAH) PWM0 channel 2 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH2_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH2_CNT_H	Channel 2 count configuration register high 8 bits. Configure PWM output duty cycle.

PWM0_CH3_CNT_L (ABH) PWM0 channel 3 count value configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH3_CNT_L	Channel 3 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_CH3_CNT_H (ACH) PWM0 channel 3 count value configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_CH3_CNT_H							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_CH3_CNT_H	Channel 3 count configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_MOD_L (ADH) PWM0 cycle configuration register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_L							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PWM0_MOD_L	PWM0 count cycle configuration register low 8 bits. Configure PWM output duty cycle.

PWM0_MOD_H (AEH) PWM0 cycle configuration register high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM0_MOD_H							
R/W	R/W							
Reset value	0							

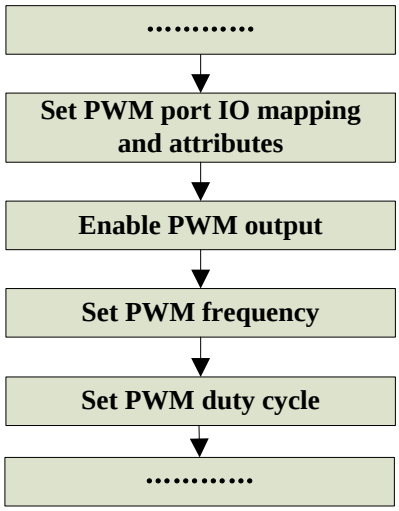
Bit number	Bit symbol	Description
7~0	PWM0_MOD_H	PWM0 count cycle configuration register high 8 bits. Configure PWM output duty cycle.

PWM_IO_SEL(B2H) PWM channel selection IO configuration register

Bit number	7	6	5	4
Symbol	-	-	PWM2_CH_SEL	PWM1_CH_SEL
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	PWM0_CH3_SEL	PWM0_CH2_SEL	PWM0_CH1_SEL	PWM0_CH0_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5	PWM2_CH_SEL	PWM2 channel selection IO port configuration 0: PD1 port selects PWM2 function; 1: PC7 port selects PWM2 function
4	PWM1_CH_SEL	PWM1 channel selection IO port configuration 0: PD0 port selects PWM1 function; 1: PC6 port selects PWM1 function
3	PWM0_CH3_SEL	PWM0 channel 3 select IO port configuration 0: PB3 port selects PWM0_CH3 function; 1: PC5 port selects PWM0_CH3 function
2	PWM0_CH2_SEL	PWM0 channel 2 selects IO port configuration 0: PB2 port selects PWM0_CH2 function; 1: PC3 port selects PWM0_CH2 function
1	PWM0_CH1_SEL	PWM0 channel 1 select IO port configuration 0: PB1 port selects PWM0_CH1 function; 1: PC0 port selects PWM0_CH1 function
0	PWM0_CH0_SEL	PWM0 channel 0 select IO port configuration 0: PB0 port selects PWM0_CH0 function; 1: PB5 port selects PWM0_CH0 function

11.5. PWM Configure Process



PWM configure process

PWM0 configuration process:

1. Configure the channel control register PWM0_CH_CTRL (channel enable and polarity selection);
2. Configure the enable register PWM0_EN, configure the count register PWM0_CHn_CNT_L/H, and the period register PWM0_MOD_L/H (the last configuration) to start working.

Note:

1. The period and duty cycle registers need to be configured when PWM0_EN=1. The counting register PWM0_CHn_CNT_L/H and the period register PWM0_MOD_L/H (update the duty cycle and period) are allowed to be configured during operation, and they are allowed to be in the same cycle Multiple channels are updated at the same time. The channel control register PWM0_CH_CTRL is not allowed to be configured during the update period. The channel control register PWM0_CH_CTRL can be changed only when PWM0_EN=0. When PWM0_EN=1, writing the count register and period configuration register will directly update the duty cycle and period. During the counter operation, the write count register and period configuration register will be latched, and the register value will be updated when the counter (PWM0_MOD) becomes (PWM0_MOD+1), that is, the duty cycle and period will be updated after a complete period.
2. Frequency range: 184 Hz~120 kHz is recommended.

12. Touch Key

CSD features:

- CSD charge and discharge clock three modes are optional:
  - Fixed frequency division of the system clock 12M~193k
  - PRS 1.5M normal distribution
  - PRS 3.5M normal distribution
- CSD count clock 24M, 12M, 6M, 4M is optional;
- Counting width 9-16 bits optional;
- Support asynchronous scanning mode;
- Support wake up in wait mode

The BF7412AMXX-XJLX implements multiple functions through a series of register.The relationship between the capactitance detection related quantity and the SFR value is as follows:

The count value is proportional to RESO, Rb resistance, PULL_I_SELA_H, and inversely proportional to VTH_SEL. In the case of ensuring complete charge and discharge, it is proportional to the charge and discharge frequency set by PRS_DIV.

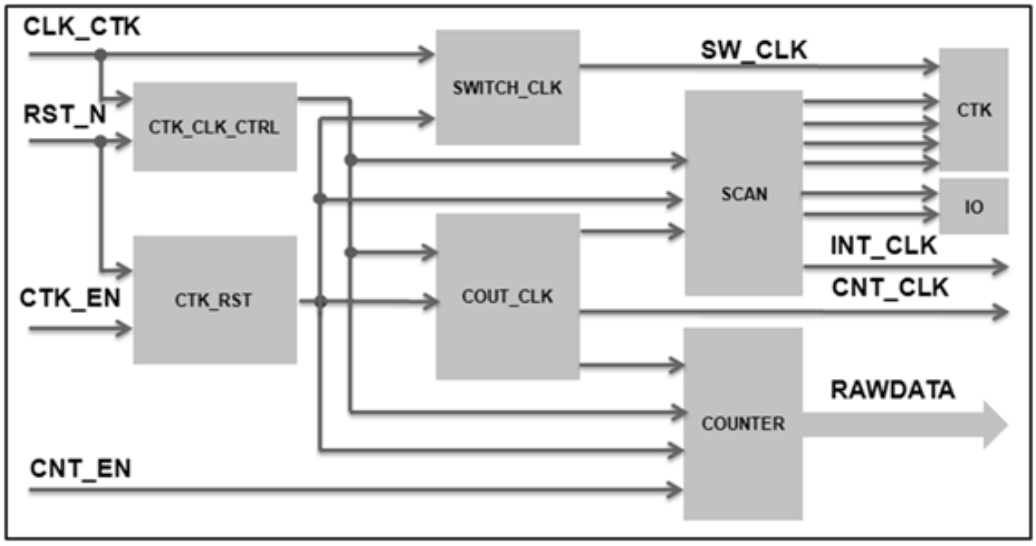
Channel touch variation is proportional to RESO and Rb, and inversely proportional to VTH_SEL. In the case of ensuring complete charge and discharge. Compared with the charge and disarge frequency set by PRS_DIV and the amount of touch change.

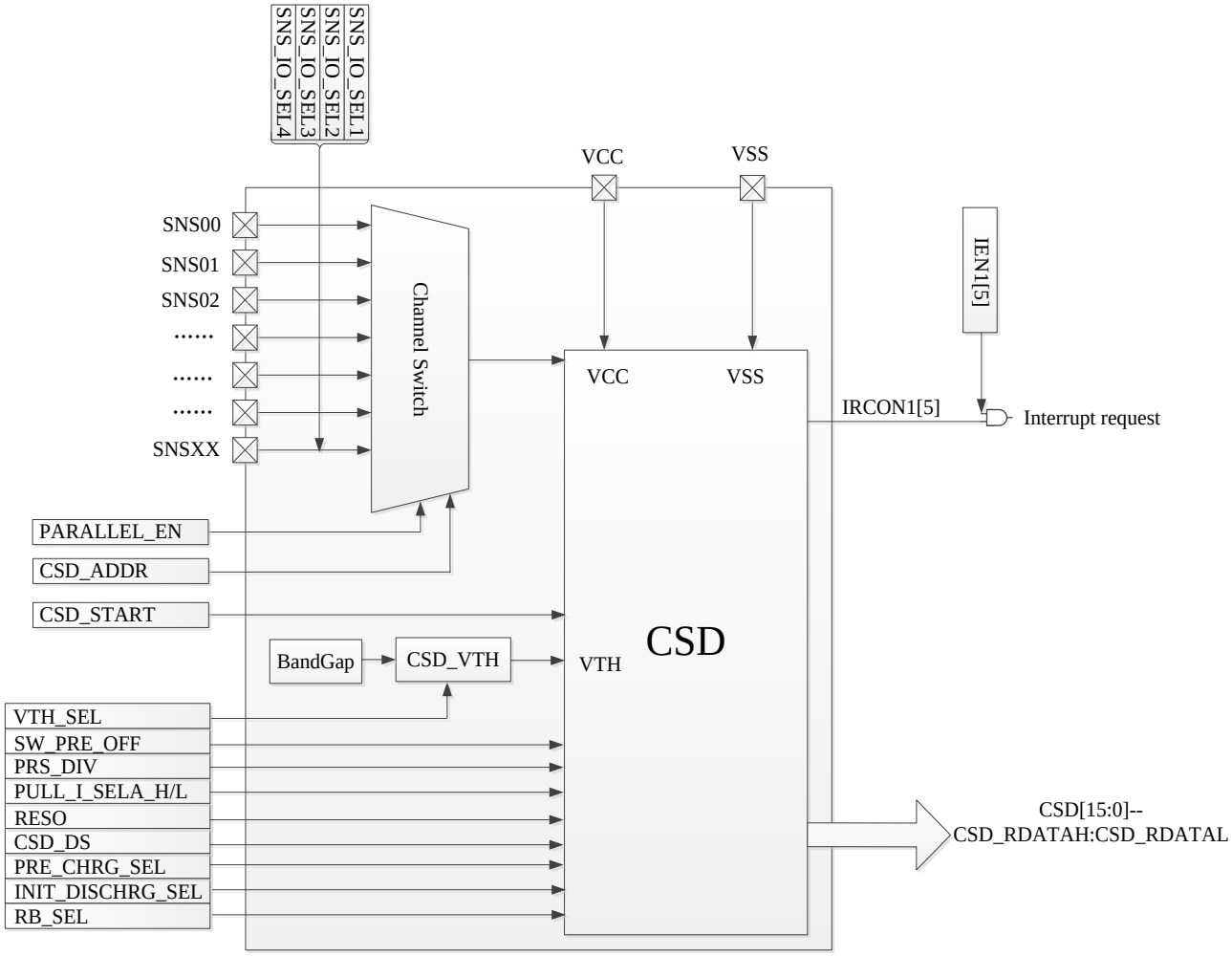
The signal-to-noise ratio of touch is proportional to VTH_SEL and PULL_I_SELA_L, and inversely proportional to CSD_DS. When the charge and discharge are incomplete, it is inversely proportional to the charge-discharge frequency set by PRS_DIV and the signal-to-noise ratio.

The time for a signal touch key detection is related to RESO and CSD_DS.

Notes: When configuring parameters, ensure that the touch key is fully charged and discharged.

CSD module structure diagram





CSD structure diagram

12.1. Touch Key Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xCA	CSD_START	RW	xxxx_xxx0b	CSD scan open register
0xCB	SNS_SCAN_CFG1	RW	x000_0000b	Touch key scan configuration register 1
0xCC	SNS_SCAN_CFG2	RW	x100_0000b	Touch key scan configuration register 2
0xCD	SNS_SCAN_CFG3	RW	x111_0000b	Touch key scan configuration register 3
0xCE	CSD_RAWDATAL	R	0000_0000b	CSD counter, low 8-bit
0xCF	CSD_RAWDATAH	R	0000_0000b	CSD counter, high 8-bit
0xD1	PULL_I_SELA_L	RW	0000_0000b	CSD pull-up current source selection register
0xD2	SNS_ANA_CFG	RW	xx10_1101b	CSD scan parameter configuration register
0xD3	SNS_IO_SEL1	RW	0000_0000b	SNS channel select register 1
0xD4	SNS_IO_SEL2	RW	0000_0000b	SNS channel select register 2
0xD5	SNS_IO_SEL3	RW	0000_0000b	SNS channel select register 3
0xD6	SNS_IO_SEL4	RW	xxxx_xx00b	SNS channel select register 4
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xxxx_0111b	Module switch control register

CSD registers list

12.2. Touch Key Register Detailed Description

CSD_START(CAH) CSD scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	1: CSD scanning is on; 0: CSD scan stops Write 1 in CSD_START to start scanning. After one scan, the hardware will automatically set to 0. If you want to start the next scan, you need to set it to 1 again by software; if CSD_START=0 during the scan, the scan will stop immediately, and the module will have related internal signals Reset

		Note: Must be used in accordance with the process configuration: CSD_START=1, if interruption is detected, configure CSD_START=0. CSD_START is not allowed to be configured during scanning

SNS_SCAN_CFG1 (CBH) Touch key scan configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	SW_PRE_OFF	PRS_DIV					
R/W	-	R/W	R/W					
Reset value	-	0	0					

Bit number	Bit symbol	Description
6	SW_PRE_OFF	Front-end charge and discharge clock switch control. 1: close sw_clk; 0: open sw_clk
5~0	PRS_DIV	Front-end charge and discharge clock frequency selection register: 0~61: fixed frequency: F=F24m/2/(PRS_DIV+4) (12M~193K); 62: highest frequency 4M, lowest frequency 1M, center frequency 1.5M, normal distribution; 63: highest frequency 4M, lowest frequency 1M, center frequency 1.5M, normal distribution.

SNS_SCAN_CFG2 (CCH) Touch key scan configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	PULL_I_SELA_H	PARALLEL_EN	CSD_ADDR				
R/W	-	R/W	R/W	R/W				
Reset value	-	1	0	0				

Bit number	Bit symbol	Description
6	PULL_I_SELA_H	CSD pull-up current source configuration highest bit.
5	PARALLEL_EN	SNS channel shunt enable register. 1: multi-channel parallel; 0: signal channel.
4~0	CSD_ADDR	The address of the detection channel 0~25 corresponds to the channel number 0~25

SNS_SCAN_CFG3(CDH) Touch key scan configuration register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-	RESO			CSD_DS		PRE_CHRG_SEL	INIT_DISCHRG_SEL
R/W	-	R/W			R/W		R/W	R/W
Reset value	-	1	1	1	0	0	0	0

Bit number	Bit symbol	Description
6~4	RESO	Counter bit select register. 000: 9 bits; 001: 10 bits; 010: 11 bits; 011: 12bits; 100: 13 bits; 101: 14 bits; 110: 15 bits; 111: 16 bits.
3~2	CSD_DS	Count clock frequency selection register. 00: 24M; 01: 12M; 10: 6M; 11: 4M; default 0.
1	PRE_CHRG_SEL	Pre-charge time selection 0: 20μs; 1: 40μs.
0	INIT_DISCHRG_SEL	Pre-discharge time selection 0: 2μs; 1: 10μs.

CSD_RAWDATAL (CEH) CSD counter, low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	RAWDATA<7:0>							
R/W	R							
Reset value	0							

CSD_RAWDATAH (CFH) CSD counter, high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	RAWDATA<15:8>							
R/W	R							
Reset value	0							

PULL_I_SELA_L (D1H) CSD pull-up current source selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	PULL_I_SEL<7:0>							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	PULL_I_SEL<7:0>	CSD pull up current source size selection switch. The default is 0.

SNS_ANA_CFG (D2H) CSD scan parameter configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	RB_SEL			VTH_SEL		
R/W	-	-	R/W			R/W		
Reset value	-	-	1	0	1	1	0	1

Bit number	Bit symbol	Description
5~4	RB_SEL	Rb resistance size selection.

		100: 60k; 101: 80k; Other: reserved Need to read Rb80k calibration value from chip flash when using: CBYTE [0x401E] k/80k, proportional calculation normalization sensitivity.
2~1	VTH_SEL	VTH voltage selection signal 000: 1.4V, 001: 2.1V; 010: 2.5V; 011: 2.8V; 100: 3.2V; 101: 3.5V; 110: 3.9V; 111: 4.1V.

SNS_IO_SEL1(D3H) SNS channel select register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL1 [7:0]	SNS_IO_SEL1 [7:0] corresponds to SNS7~SNS0. The corresponding bit is 1: select SENSOR enable; 0: do not select SENSOR enable

SNS_IO_SEL2 (D4H) SNS channel select register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL2 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL2 [7:0]]	SNS_IO_SEL2[7:0] corresponds to SNS15~SNS8. The corresponding bit is 1: Select SENSOR to enable; 0: Do not select SENSOR enable

SNS_IO_SEL3 (D5H) SNS channel select register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	SNS_IO_SEL3 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SNS_IO_SEL3 [7:0]	SNS_IO_SEL3 [7:0] corresponds to SNS23~SNS16.

		The corresponding bit is 1: Select SENSOR to enable; 0: Do not select SENSOR enable

SNS_IO_SEL4 (D6H) SNS channel select register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	SNS_IO_SEL4[1:0]
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
1~0	SNS_IO_SEL4[1:0]	SNS_IO_SEL4[1:0] corresponds to SNS25~SNS24. The corresponding bit is 1: select SENSOR enable; 0: Do not select SENSOR enable

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	EX5	CSD interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	IE5	CSD interrupt flag 1: There is a CSD interrupt flag; 0: No CSD interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
5	IPL1.5	CSD interrupt priority. 0: low priority; 1: high priority

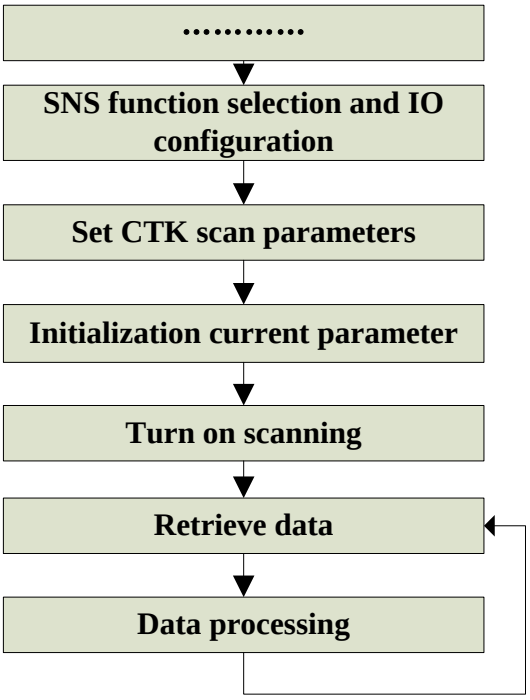
PD_ANA (FEH) Module switch control register

Bit number	7~4	3	2	1	0
Symbol	-	PD_OSC_32K	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	1	1	1

Bit number	Bit symbol	Description
1	PD_CSD	Analog CSD work control register: 0: CSD module works normally; 1: CSD module does not work

12.3. Touch Key Configure Process

CTK touch key scan for query or interrupt mode. At first, configuring the CTK scanning parameter. Second, starting CTK scanning; Then obtain and save CTK data at CTK interrupt, software algorithm for data processing and touch key output judgement.



CTK configure process

Through the sensitivity parameter configuration, a set of parameters with better signal-to-noise ratio is obtained, thereby improving the accuracy of the key judgment.

1. **RESO:** 0~7 CTK capacitiance scanning resolution, counter digits: **(RESO + 9)bit,** the bigger CTK scanning resolution, the bigger the downward rawdata, the noise is increased at the same time, conversely reverse.
2. **VTH_SEL:** 0~7, the lower VTH, the bigger raw data, the noise is increased at the same time, conversely reverse.
3. **CSD_DS:** Detect speed **0: 24M, 1: 12M, 2: 6M, 3: 4M,** the slower detect speed the slower raw data simple time, conversely reverse. Suggest default 24M, at least twice the speed of the PRS clock.
4. **RB_SEL:** Rb resistance select: **4: 60k, 5: 80k**; The greater resistance, the bigger raw data, the noise is increased at the same time, conversely reverse.
5. **PRS_DIV:** front-end charge and discharge clock frequency selection register:
   0~61: fixed frequency: F=F24m/2/(PRS_DIV+4) (12M~193k);
   62: the highest frequency 4M, the lowest frequency 1M, center frequency 1.5M, normal distribution;
   63: the highest frequency 4M, the lowest frequency 1M, center frequency 1.5M, normal distributed;
   The larger the PRS clock, the larger the amount of charge in Rawdata, and the greater the noise introduced, and vice versa.
6. **PULL_I_SELA_L:** pull-up current source low 8 bit.
7. **PULL_I_SELA_H:** pull-up current source high bit, default: 0x01.
   Current resources value =255.5-0.5*{PULL_I_SELA_H, PULL_I_SELA_L}, the smaller the current source, the smaller the count value, default: 0x00.

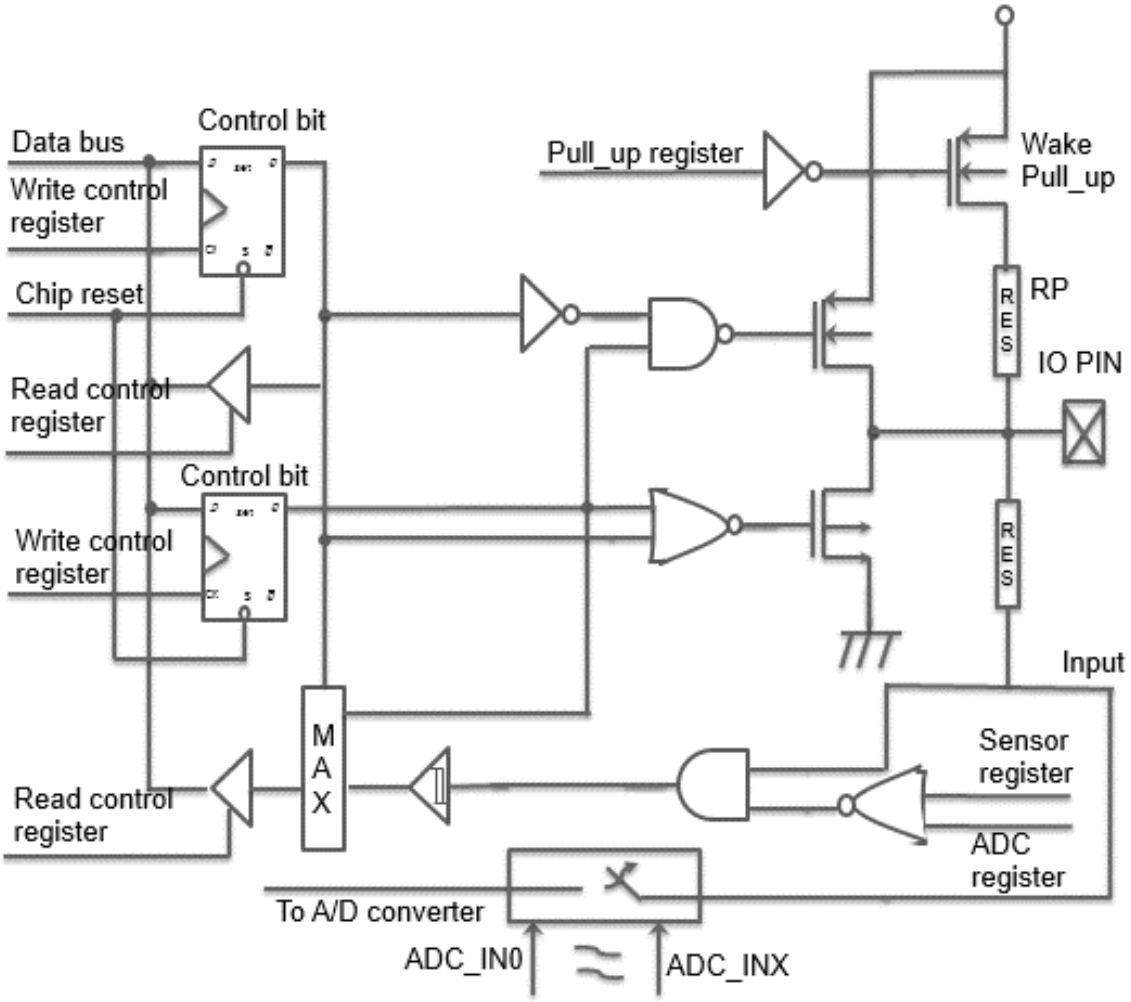
Notes:

1. **Rawdata is the real-time raw count value of the CTK capacitor counter.**
2. **In practical applications, it is necessary to view the data through the programming software and compare the parameters with good signal-to-noise ratio.**
3. **Chip supply voltage and reference voltage: VCC-VTH>0.5V.**

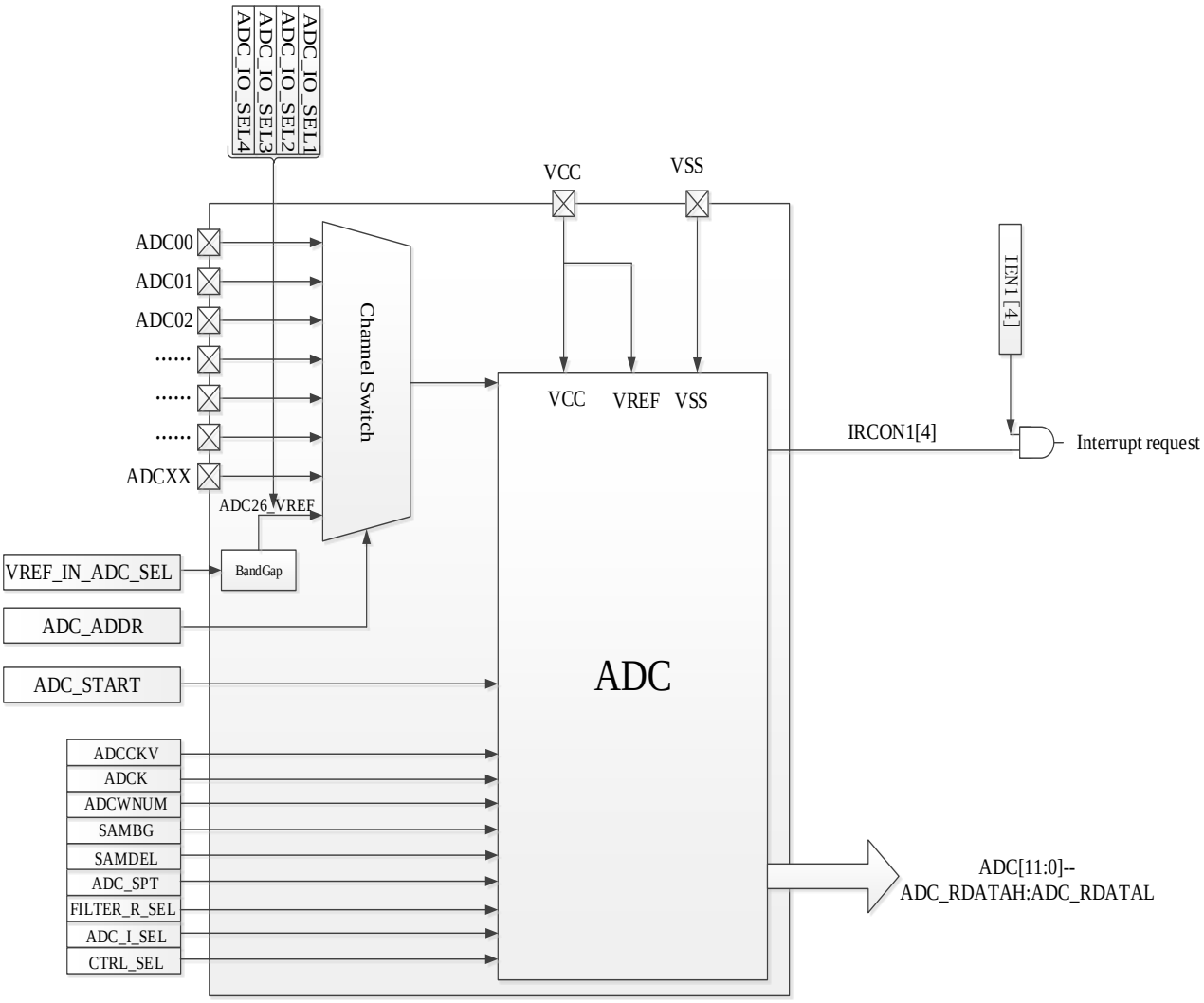
13. ADC

The BF7412AMXX-XJLX chip include a signal-ended, 12-bit linear successive approximation analog -to-digital converter (ADC). The reference voltage of the ADC is connected to the VCC of the chip. ADC channels can input independent analog signals. ADC module converts one channel at a time, ADC_START=0→1(⎍) turn on conversion. Update the ADC result register and generate an interrupt after the conversion is complete. The ADC module has the following characteristics:

- Liner successive approximation ADC with 12bit resolution;
- Single conversion mode;
- Sampling time and conversion speed are configurable;
- Support wake up in wait mode



ADC schematic



ADC block diagram

13.1. ADC Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xB4	ADC_SPT	RW	0000_0000b	ADC sampling time configure register
0xB5	ADC_SCAN_CFG	RW	xx00_0000b	ADC scan control register
0xB6	ADCCKC	RW	xxxx_0000b	ADC clock control register
0xB9	ADC_RDATAH	R	xxxx_0000b	ADC scan result register, high 4 bit.
0xBA	ADC_RDATAL	R	0000_0000b	ADC scan result register, low 8 bit.
0xBB	ADC_CFG1	RW	0000_0000b	ADC sampling time configure register 1
0xBC	ADC_CFG2	RW	xx00_0111b	ADC sampling time configure register 2
0xD9	ADC_IO_SEL1	RW	0000_0000b	ADC function select register 1
0xDA	ADC_IO_SEL2	RW	0000_0000b	ADC function select register 2
0xDB	ADC_IO_SEL3	RW	0000_0000b	ADC function select register 3
0xDC	ADC_IO_SEL4	RW	xxxx_xx00b	ADC function select register 4
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFE	PD_ANA	RW	xxxx_0111b	Module switch control register

ADC registers list

13.2. ADC Register Details

ADC_SPT (B4H) ADC sample time configure register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT	ADC sample time configure register sample time: sample_Timer = (ADC_SPT+1)*4Tadc_clk

ADC_SCAN_CFG (B5H) ADC scan control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	ADC_ADDR					ADC_START
R/W	-	-	R/W					R/W
Reset value	-	-	0					0

Bit number	Bit symbol	Description
5~1	ADC_ADDR	ADC channel address selection register 00000: corresponds to ADC0; 00001: corresponding to ADC1; ... 11001: corresponding to ADC25; 11010: ADC26_VREF; Other values: reserved
0	ADC_START	ADC scan enable register 0: ADC module does not scan; 1: ADC module starts scanning ADC_START is set from 0 to 1, ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit, the ADC interrupt flag bit needs to be cleared by software Note: ADC_START is not allowed to be configured during scanning

ADCCKC (B6H) ADC clock control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADCCKV		ADCCK	
R/W	-	-	-	-	R/W		R/W	
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3~2	ADCCKV	ADC comparator offset cancellation analog input clock. 0: 12MHz 1: 6MHz 2: 3MHz 3: 2MHz
1~0	ADCCK	ADC_CLK frequency division selection. 0: 3MHz 1: 2MHz 2: 1.5MHz 3: 1MHz

ADC_RDATAH (B9H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RAWDATA<11:8>			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

Bit number	Bit symbol	Description
3~0	ADC_RAWDATA<11:8>	ADC scan result register

ADC_RDATAL(BAH) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RAWDATA<7:0>							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_RAWDATA<7:0>	ADC scan result register

ADC_CFG1(BBH) ADC sampling timing control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADCWNUM					SAMBG	SAMDEL	
R/W	R/W					R/W	R/W	
Reset value	0					0	0	

Bit number	Bit symbol	Description
7~3	ADCWNUM	Selection of distance conversion interval after sampling 3+ADCWNUM(ADC_CLK)
2	SAMBG	Sampling timing and comparison timing interval selection 0: interval 0; 1: interval 1 (ADC_CLK)
1~0	SAMDEL	Sampling delay time selection 0:0; 1:2; 2:4; 3:8 (ADC_CLK)

ADC_CFG2 (BCH) ADC sampling timing control register 2

Bit number	7	6	5	4
Symbol	-	-	VREF_IN_ADC_SEL	

R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	FILTER_R_SEL	ADC_I_SEL		CTRL_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	1	1	1

Bit number	Bit symbol	Description
5~4	VREF_IN_ADC_SEL	ADC26 internal input voltage selection 00: 1.378V; 01: 2.271V; 10: 3.168V; 11: 4.06V
3	FILTER_R_SEL	Input signal filter selection 0 means no RC filter, 1 means RC filter
2	ADC_I_SEL[1]	ADC bias current size selection register Op amp bias current selection signal 0 is 1uA; 1 is 2uA
1	ADC_I_SEL[0]	ADC bias current size selection register Comparator bias current selection signal 0 is 1uA; 1 is 2uA
0	CTRL_SEL	ADC comparator offset cancellation selection signal 0: First sampling and then offset elimination; 1: All switches are disconnected together

ADC_IO_SEL1 (D9H) ADC function selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1[7:0]	ADC_IO_SEL1[7:0] corresponds to ADC07~ADC00. The corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL2(DAH) ADC function selection register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description

7~0	ADC_IO_SEL2[7:0]	ADC_IO_SEL2[7:0] corresponds to ADC15~ADC08. The corresponding bit is 1: Select ADC function; 0: Do not select ADC function

ADC_IO_SEL3(DBH) ADC function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3[7:0]	ADC_IO_SEL3[7:0] corresponds to ADC23~ADC16. The corresponding bit is 1: select ADC function; 0: The ADC function is not selected

ADC_IO_SEL4(DCH) ADC function selection register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADC_IO_SEL4[1:0]	
R/W	-	-	-	-	-	-	R/W	
Reset value	-	-	-	-	-	-	0	

Bit number	Bit symbol	Description
1~0	ADC_IO_SEL4[1:0]	ADC_IO_SEL4[1:0] corresponds to ADC25~ADC24. The corresponding bit is 1: Select ADC function; 0: Do not select ADC function

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	EX4	ADC interrupt enable 1: interrupt enable; 0: interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	IE5	IE4	IE3	IE2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-

Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	IE4	ADC interrupt flag 1: There is a ADC interrupt flag; 0: No ADC interrupt flag

IPL1 (F6H) Interrupt priority register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
4	IPL1.4	ADC interrupt priority. 0: low priority; 1: high priority

PD_ANA (FEH) Module switch control register

Bit number	7~4	3	2	1	0
Symbol	-	PD_OSC_32K	PD_XTAL_32K	PD_CSD	PD_ADC
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	1	1	1

Bit number	Bit symbol	Description
0	PD_ADC	Analog ADC shutdown control register 0: ADC module works normally; 1: ADC module does not work

Note:

ADC detection time:

Formula	**Description**
$T_{AD}=T_{ADC\_SPT}+T_{W1}+T_{W2}$	ADC conversion time
$T_{ADC\_SPT(\mu s)} = 4*(ADC\_SPT+1) *T_{adc\_clk}$	ADC sampling time
$T_{W1}=(ADCWNUM+3+ SAMDEL)*T_{adc\_clk}$	Distance conversion internal after sampling and delay time
$T_{W2}=(2*1+12)*T_{adc\_clk}$	Fixed time

1. **Timing requirements**: (3+ADCWNUM)/F_ADCK >4 /F_ADCCKV;
   F_ADCK: ADC frequency division clock;
   F_ADCCKV: ADC comparator offset cancellation analog input clock;
   ADC external signal plus RC filtered voltage setting time >= 2*(ADC sampling converts time);
2. When the power supply voltage fluctuates greatly or drops, the VCC voltage value can be calculated by the formula ADCINNER_Data/VREF_IN_ADC_SEL = 4096/VCC, and the Vin voltage value can be calculated by the formula Vin_Data/Vin=4096/VCC.
   ADCINNER_Data: ADC internal channel data
   Vin_Data: ADC input channel data
   Vin: input voltage
   VREF_IN_ADC_SEL: need to read the chip calibration value
   Vin = (Vin_Data/ADCINNER_Data)*VREF_IN_ADC_SEL. First obtain the internal channel data, and then obtain the input voltage Vin_Data data, and the interval between the two acquisitions should be as short as possible.
3. **ADC interrupt conditions**: the configuration sequence is ADC_IO_SEL enable -> ADC interrupt enable -> ADC_ADDR (the address must correspond to ADC_IO_SEL) -> ADC_START. Pay attention to the initial configuration timing during application. If there is an application where the ADC and IO port functions are multiplexed, you need to pay attention to the switching timing. If the ADC_IO_SEL enable is turned off or the address does not correspond to ADC_IO_SEL, the ADC scan cannot be turned on. The configuration sequence must be followed: ADC_IO_SEL enable -> ADC interrupt enable -> ADC_ADDR (the address must correspond to ADC_IO_SEL) -> ADC_START sequence to start ADC scanning.
4. CBYTE[0x4020] = ADC internal channel input voltage calibration value, high eight bits,
   CBYTE[0x4021] = ADC internal channel input voltage calibration value, low eight bits,
   Read the 1.378V calibration value of the ADC internal channel input voltage of the chip information address;

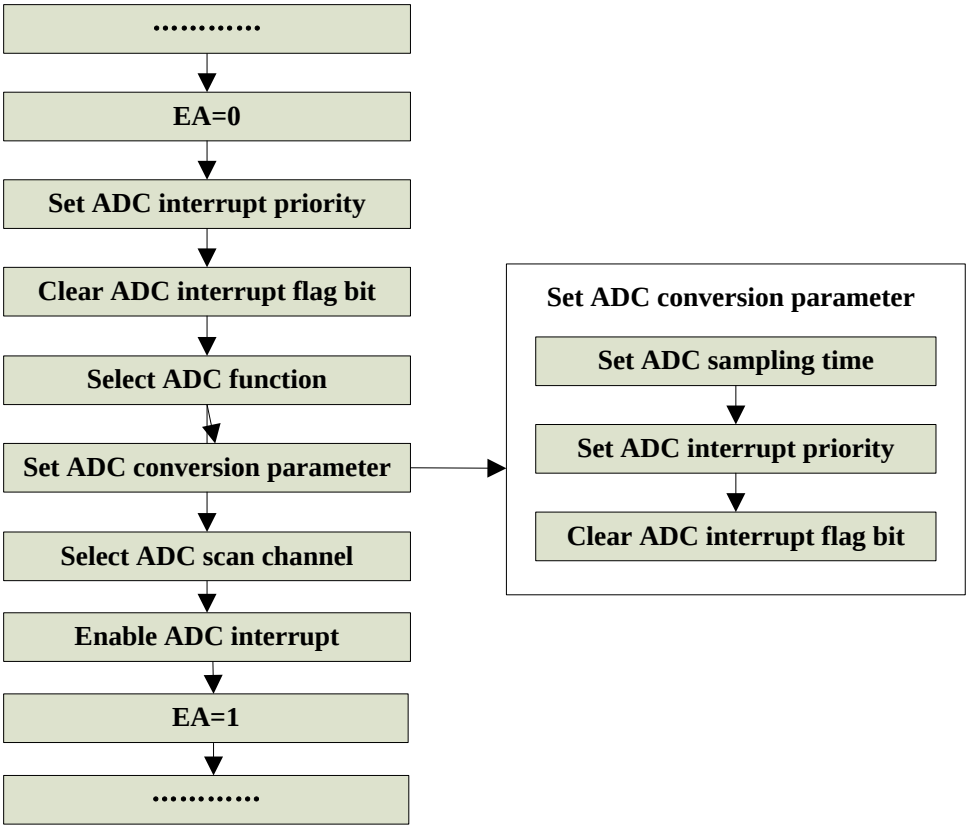
   CBYTE[0x4022] = ADC internal channel input voltage calibration value, high eight bits,
   CBYTE[0x4023] = ADC internal channel input voltage calibration value, low eight bits,
   Read the 2.271V calibration value of the ADC internal channel input voltage of the chip information address;

CBYTE[0x4024] = ADC internal channel input voltage calibration value, high eight bits,
CBYTE[0x4025] = ADC internal channel input voltage calibration value, low eight bits,
Read the3.168V calibration value of the ADC internal channel input voltage of the chip information address;

CBYTE[0x4026] = ADC internal channel input voltage calibration value, high eight bits,
CBYTE[0x4027] = ADC internal channel input voltage calibration value, low eight bits,
Read the 4.06V calibration value of the ADC internal channel input voltage of the chip information address;

6. When the pin is configured as ADC function, the pin needs to be configured as IO input mode, and other multiplexing functions are turned off, such as pull-up resistors, etc.

13.3. ADC Configuration Process



ADC configuration process

14. LVDT

The BF7412AMXX-XJLX supports low pressure alarm function, effectively monitor voltage dynamics. Support 5 levels of voltage: 3.0V/3.3V/3.6V/3.9V/4.2V (Preset point buck interrupt, hysteresis 0.1V to generate corresponding boost interrupt).

When the voltage monitoring configures the above threshold, the voltage drops to this threshold will trigger a low voltage interrupt. The system can be propely processed in low voltage interrupts according to the needs of the application.

14.1. LVDT Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Description**
0x86	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/LVDT buck interrupt status register
0xB3	LVDT_SEL	RW	xx11_1000b	LVDT control register
0xE1	IRCON2	RW	xxxx_x000b	Interrupt flag register 2
0xE7	IEN2	RW	xxxx_x000b	Interrupt enable register 2
0xF4	IPL2	RW	xxxx_x000b	Interrupt priority register 2

LVDT register list

14.2. LVDT Register Detailed Description

INT_POBO_STAT (86H) LVDT boost/LVDT buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	Lvdt boost interrupt status 1: boost interrupt is valid 0: boost interrupt is invaild
0	INT_BO_STAT	Lvdt buck interrupt state 1: buck interrupt is valid 0: buck interrupt is invalid

LVDT_SEL(B3H) LVDT control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	PD_LVDT	SEL_LVDT_DELAY		SEL_LVDT_VTH		

R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	1	1	1	0	0	0

Bit number	Bit symbol	Description
5	PD_LVDT	LVDT control register 1: close; 0: open, close by default
4~3	SEL_LVDT_DELAY	Select signal, select LVDT power-down delay; default 11 0: Delay time 1; 1: Delay time 2; 2: Delay time 3; 3: Delay time 4
2~0	SEL_LVDT_VTH	LVDT threshold selection 000/001: reserved; 010: 3.0V; 011: 3.3V; 100: 3.6V; 101: 3.9V; 11x: 4.2V

SEL_LVDT_VTH	SEL_LVDT_DELAY	LVDT			
		Power down threshold (V)	Recovery threshold (V)	Hysteresis (mV)	Delay (μs)
010	00	3.0	3.1	117	8.0
	01	3.0	3.1	118	15.8
	10	3.0	3.1	118	34.7
	11	3.0	3.1	120	63.0
011	00	3.3	3.4	93	8.6
	01	3.3	3.4	94	17.0
	10	3.3	3.4	95	34.0
	11	3.3	3.4	97	68.0
100	00	3.6	3.7	110	9.1
	01	3.6	3.7	110	18.1
	10	3.6	3.7	111	36.3
	11	3.6	3.7	113	72.5
101	00	3.9	4.1	131	9.6
	01	3.9	4.1	132	19.2
	10	3.9	4.1	133	38.5
	11	3.9	4.1	135	77.0
11X	00	4.2	4.3	124	10.0
	01	4.2	4.3	125	20.0
	10	4.2	4.3	126	40.0
	11	4.2	4.3	128	80.0

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IE10	IE9	IE8

R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
0	IE8	LVDT interrupt flag 1: There is a LVDT interrupt flag; 0: No LVDT interrupt flag

IEN2(E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	EX10	EX9	EX8
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

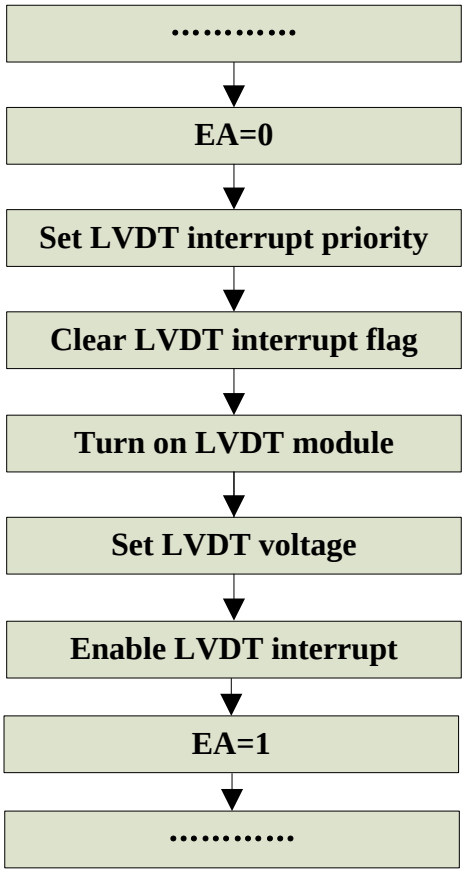
Bit number	Bit symbol	Description
7~3	-	Reserved
2	EX10	UART1 interrupt enable 1: interrupt enable; 0: interrupt disable
1	EX9	UART0 interrupt enable 1: interrupt enable; 0: interrupt disable
0	EX8	LVDT interrupt enable 1: interrupt enable; 0: interrupt disable

IPL2 (F4H) Interrupt priority register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	IPL2.2	IPL2.1	IPL2.0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
0	IPL2.0	LVDT interrupt priority. 0: low priority; 1: high priority

14.3. LVDT Configuration Process



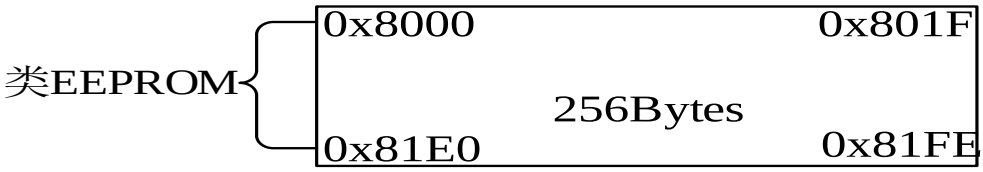
LVDT Configuration Process

15. EEPROM

EEPROM size is 256 Bytes, which can be divided into 16 pages, each page is 16 Bytes.

EEPROM address is 0x8000+2*i (i = 0x00~0xFF). Page erasure is required when using, then perform byte write operation, and can only be written once after erasing.

The data erased by EEPROM is indeterminate.



EEPROM address

15.1. EEPROM Related Register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0xFA	SPROG_ADDR_L	RW	0000_0000b	EEPROM address control register
0xFB	SPROG_DATA	RW	xxxx_0000b	EEPROM data register
0xFC	SPROG_CMD	RW	0000_0000b	EEPROM command register
0xFD	SPROG_TIM	RW	xxxx_0001b	EEPROM erase time control register

EEPROM registers list

15.2. EEPROM Register Detailed Description

SPROG_ADDR_L(FAH) EEPROM address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	EEPROM block address low 8 bits SPROG_ADDR_L [3:0]: select the address in the page, SPROG_ADDR_L [7:4]: select the page.

SPROG_DATA(FBH) EEPROM data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	EEPROM programming: the number of data to be written (SPROG_NUM*2bytes). When SPROG_NUM=0, it means that only 1 data is programmed

SPROG_CMD(FCH) EEPROM command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: EEPROM page erase; Write 0x69: EEPROM byte programming

SPROG_TIM (FDH) EEPROM erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset value	–	–	–	–	0	0	1	0

Bit number	Bit symbol	Description
7~4	--	Reserved
3~2	--	0~3 data writing time=1.50~2.25ms (step 0.25ms) 00: Data writing time=1.50ms; 01: Data writing time = 1.75ms; 10: Data writing time=2.00ms; 11: Data writing time = 2.25ms Note: The time for writing a single word or multiple words is the time selected above
1~0	--	0~3 page erasing time=2.25~3.00ms (step 0.25ms) 00: page erasing time = 2.25ms; 01: Page erasing time=2.50ms; 10: Page erase time=2.75ms; 11: Page erase time=3.00ms

15.3. Page Erase Step

1. SPROG_TIM[4:0] = 0~3 (3 ms recommended). Only configure once in the main program main() function initialization;
2. Turn off the interrupt;
3. Configure SPROG_ADDR_L[7:4], select the page to be erased;
4. Configure SPROG_CMD = 0x96;
5. Write 4 NOP instructions;
6. Start erasing, the CPU turns off the clock F_sys_clk, and turns on the clock F_sys_clk after erasing is completed;
7. Need to continue to erase data, skip to step 2;
8. Configure SPROG_ADDR_L=0x00, restore interrupt settings

15.4. Byte Write Step

1. Prepare EEPROM to write cache data, the cache address is xram address 0x00+2*i(i=0~15);
2. SPROG_TIM[3:2] = 0~3 (recommended 2.25ms), only configure once in the main program main() function initialization;
3. Turn off the interrupt;
4. Configure SPROG_ADDR_L[3:0] and select the first address of the page corresponding to SPROG_ADDR_L[7:4];
5. Configure SPROG_NUM, select the number of characters to be programmed (0~15) (when SPROG_NUM=0, it means that only 1 data is programmed);
6. Configure SPROG_CMD = 0x69;
7. Write 4 NOP instructions;
8. Start programming, the CPU turns off the clock F_sys_clk, and then turns on the clock F_sys_clk after completion;
9. Need to continue programming data, skip to step 3;
10. Configure SPROG_ADDR_L=0x00 to restore interrupt settings.

NOTE:

1. The data written in EEPROM is read from xram address (0x00+2*i(i=0~15)).
2. When SPROG_NUM =0~15, it means that the number of bytes to be programmed is SPROG_NUM +1. When {SPROG_ADDR_L[3:0]+ SPROG_NUM}>15, for the excess part, the programmed data will overwrite the original data starting from the top address of the page.
   For example, SPROG_ADDR_L[7:0]=0x0a; SPROG_NUM=10; the number of bytes that need to be programmed is 11; at this time, the six address spaces of 0x8014, 0x8016, 0x8018, 0x801A, 801C, and 0x801E are programmed normally, but There are still 5 bytes

that have not been programmed. At this time, the remaining 5 data will be programmed into the 5 address spaces of 0x8000, 0x8002, 0x8004, 0x8006, and 0x8008.

15.5. Address Correspondence

EEP page	Page erase logical address SPROG_ADDR_L [7:4] (HEX)	Page erase physical address (HEX)
0	00	8000
1	01	8020
2	02	8040
3	03	8060
4	04	8080
5	05	80A0
6	06	80C0
7	07	80E0
8	08	8100
9	09	8120
10	0A	8140
11	0B	8160
12	0C	8180
13	0D	81A0
14	0E	81C0
15	0F	81E0

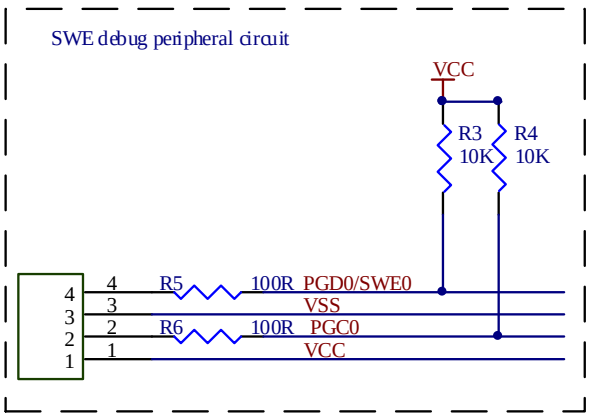
EEP page	Address in EEP page SPROG_ADDR_L [3:0](HEX)	Data write logical address SPROG_ADDR_L [7:0] (HEX)	Data write physical address (HEX)
0	00	00	8000
0	01	01	8002
0	02	02	8004
0	03	03	8006
…	…	…	…
0	0D	0D	801A
0	0E	0E	801C
0	0F	0F	801E
1	00	10	8020
1	01	11	8022
…	…	…	…
2	00	20	8040
…	…	…	…
15	00	F0	81E0

15	01	F1	81E2
…		…	…
15	0B	FB	81F6
15	0C	FC	81F8
15	0D	FD	81FA
15	0E	FE	81FC
15	0F	FF	81FE

16. Burning and Debugging

16.1. SWE Circuit Connection

Two-wire programming and single-wire debugging. When performing simulation debugging, you need to connect a SWE wire. In the SWE debugging mode, the IO function of the SWE port is blocked. It is recommended not to configure other functions of the SWE debugging I/O port to avoid affecting the SWE debugging function.



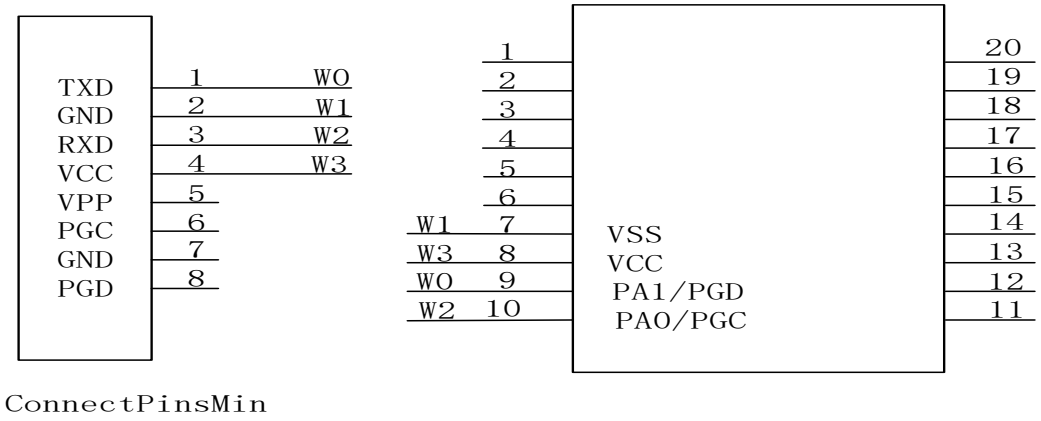
SWE circuit connection

16.2. TouchKey Programming

Connect the chip PGD, PGC, VCC, VSS four lines. When entering the programming interface, select the chip of the corresponding model. Open the compiled HEX file, click on a built-in flash to wait for burning.

When entering the debugging interface, first burn the HEX file with the debug data transmission mode, click to open the debug to view the touch key data.

For example:



BF7412AM_SOP20 burning wiring diagram

Notes: refer to the TK programming guide for specific operation instructions.

17. CPU Instruction System

17.1. Instruction Code

The BF7412AMXX-XJLX instructions are divided into signal-byte instructions, double-byte instructions and three-byte instructions.

Signal-byte instructions: A signal-byte instruction consists of 8 bit binary code. There are only instruction opcodes in the instruction, no instruction operand or instruction operand is implied in the instruction opcode. There are 49 such instructions.

Double-byte instructions: Consists of two bytes, one for opcode and the other for the operand (or operand address), stored in order in program memory. There are 46 such instructions.

Three-byte instructions: Consists of one byte of instruction opcode and two bytes of operands (or operand address). There are 16 such instructions.

17.2. Instruction Set

In order to describe the instructions conveniently, some symbols are used in the instructions. The meanings of these symbols are as follows:

addr 11	Lower 11 address
addr 16	16-bit address
direct	Direct addressing, 8-bit internal data and address (including special function registers)
bit	Bit address
#data	8-bit immediate
#data16	16-bit immediate
rel	Signed 8-bit relative displacement
n	Number 0~7
Rn	R0~R7 working registers of the current register group
i	Numbers 0, 1
Ri	Working register R0, R1
@	Register indirect addressing
←	Data transfer direction
∧	Logical "and"
∨	Logical OR
⊕	Logical "exclusive OR"
√	Affect the flag
×	No effect on the flag

CPU instruction symbol meaning table

The assembly instructions used, the function of each instruction, the number of bytes occupied, the instruction execution cycle and the impact on the corresponding flag bit are shown in the following table:

8 bit data transfer instructiion								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV A	Rn	A←(Rn)	√	×	×	×	1	1
	direct	A←(direct)	√	×	×	×	2	1
	@Ri	A←((Ri))	√	×	×	×	1	1
	#data	A←data	√	×	×	×	2	1
MOV Rn	A	Rn←(A)	×	×	×	×	1	1
	direct	Rn←(direct)	×	×	×	×	2	2
	#data	Rn←data	×	×	×	×	2	1
MOV direct1	A	direct1←(A)	×	×	×	×	2	1
	Rn	direct1←(Rn)	×	×	×	×	2	2
	direct2	direct1←(direct2)	×	×	×	×	3	2
MOV direct,	@Ri	direct←((Ri))	×	×	×	×	2	2
	#data	direct←data	×	×	×	×	3	2
MOV @Ri	A	(Ri)←(A)	×	×	×	×	1	1
	direct	(Ri)←(direct)	×	×	×	×	2	2
	#data	(Ri)←data	×	×	×	×	2	1
16 bit data transfer instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV DPTR,#data16		DPTR←data16	×	×	×	×	3	2
External data transfer and table lookup instructions								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOVX @DPTR,A		(DPTR)←(A)	×	×	×	×	1	2
MOVC A,	@A+DPTR	A←((A)+(DPTR))	√	×	×	×	1	2
	@A+PC	A←((A)+(PC))	√	×	×	×	1	2
MOVX A,	@DPTR	A←(DPTR)	√	×	×	×	1	2
Notes: The number of cycles and the number of bytes of the MOVX instruction can be configured through registers CKCON<2:0>.								

Exchange class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
XCH A,	Rn	(Rn)←(A)	√	×	×	×	1	2
	direct	(A)←(direct)	√	×	×	×	2	1
	@Ri	(A)←((Ri))	×	×	×	×	1	1
XCHD A,@Ri		(A)3~0~((Ri))3~0	√	×	×	×	1	1
SWAP A		(A)7-4~(A)3-0	√	×	×	×	1	1
Arithmetic operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
ADD A	Rn	A←(A)+(Rn)	√	√	√	√	1	1
	direct	A←(A)+(direct)	√	√	√	√	2	1
	@Ri	A←(A)+((Ri))	√	√	√	√	1	1
	#data	A←(A)+data	√	√	√	√	2	1
ADDC A	Rn	A←(A)+(Rn)+(C)	√	√	√	√	1	1
	direct	A←(A)+(direct) +(C)	√	√	√	√	2	1
	@Ri	A←(A)+((Ri)) +(C)	√	√	√	√	1	1
	#data	A←(A)+data+(C)	√	√	√	√	2	1
INC	A	A←(A)+1	√	×	×	×	1	1
	Rn	Rn←(Rn)+1	×	×	×	×	1	1
	direct	direct←(direct)+1	×	×	×	×	2	1
	@Ri	(Ri)←((Ri))+1	×	×	×	×	1	1
	DPTR	DPTR←((DPTR))+1	×	×	×	×	1	2
DA A		BCD code adjustment	√	×	√	√	1	1
SUBB A	Rn	A←(A)-(Rn)-(C)	√	×	×	×	1	1
	direct	A←(A)-(direct)-(C)	√	√	√	√	2	1
	@Ri	(A)←(A)-((Ri))-(C)	√	√	√	√	1	1
	#data	A←(A)-data-(C)	√	√	√	√	2	1
DEC	A	A←(A)-1	√	×	×	×	1	1
	Rn	Rn←(Rn)-1	×	×	×	×	1	1
	direct	direct←(direct)-1	×	×	×	×	2	1
	@Ri	(Ri)←((Ri))-1	×	×	×	×	1	1
MUL AB		BA←(A)*(B), after performing the multiplication operation, the lower byte is stored in A and the high byte	√	√	×	0	1	4

		is stored in B.						
DIV AB		A←(A)/(B) B←remainder	√	√	×	0	1	4
Notes: When the DA instruction is used, the adjustment rules are as follows: if the low 4 bits of accumulator A are greater than 9 or AC=1, then A←A+06H; if the high 4 bits of accumulator A are greater than 9 or CY=1, then A←A+60H.								
Logical operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
CLR A		A←00H	√	×	×	×	1	1
CPL A		A←($\overline{A}$)	√	×	×	×	1	1
ANL A,	Rn	A←(A)∧(Rn)	√	×	×	×	1	1
	direct	A←(A)∧(direct)	√	×	×	×	2	1
	@Ri	A←(A)∧((Ri))	√	×	×	×	1	1
	#data	A←(A)∧data	√	×	×	×	2	1
ANL direct,	A	direct←(A)∧(direct)	×	×	×	×	2	1
	#data	direct←(direct)∧data	×	×	×	×	3	2
ORL A,	Rn	A←(A)∨(Rn)	√	×	×	×	1	1
	direct	A←(A)∨(direct)	√	×	×	×	2	1
	@Ri	A←(A)∨((Ri))	√	×	×	×	1	1
	#data	A←(A)∨data	√	×	×	×	2	1
ORL direct,	A	direct←(direct)∨(A)	×	×	×	×	2	1
	#data	direct←(direct)∨data	×	×	×	×	3	2
XRL A,	Rn	A←(A)⊕(Rn)	√	×	×	×	1	1
	direct	A←(A)⊕(direct)	√	×	×	×	2	1
	@Ri	A←(A)⊕((Ri))	√	×	×	×	1	1
	#data	A←(A)⊕data	√	×	×	×	2	1
XRL direct,	A	direct←(direct)⊕(A)	×	×	×	×	2	1
	#data	direct←(direct)⊕data	×	×	×	×	3	2

Loop, shift class instruction							
Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
RL A	The content in A is rotated left by one bit.	×	×	×	×	1	1
RLC A	A content with carry left shift one bit.	√	×	×	√	1	1
RR A	The content in A is rotated right by one bit.	×	×	×	×	1	1
RRC A	A content with carry right shift one bit.	√	×	×	√	1	1
Call, return class instruction							
Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
LCALL addr16	(PC)←(PC)+3,(SP)←(PC), (PC)←addr16	×	×	×	×	3	2
ACALL addr11	(PC)←(PC)+2,(SP)←(PC), (PC10~0)←addr11	×	×	×	×	2	2
RET	(PC)←((SP))	×	×	×	×	1	2
RETI	(PC)←((SP)) return from interrupt	×	×	×	×	1	2
Transfer class instruction							
Mnemonic	Function	Impact on the flag				Number of bytes	Number of cycles
		P	OV	AC	CY		
LJMP addr16	PC←addr15~0	×	×	×	×	3	2
AJMP addr11	PC10~0←addr10~0	×	×	×	×	2	2
SJMP rel	PC←(PC)+rel	×	×	×	×	2	2
JMP @A+DPTR	PC←(A)+(DPTR)	×	×	×	×	1	2
JZ rel	PC←(PC)+2, If (A)=0, PC←(PC)+rel	×	×	×	×	2	2
JNZ rel	PC←(PC)+2, If (A)≠0, PC←(PC)+rel	×	×	×	×	2	2
JC rel	PC←(PC)+2, If (CY)=1, PC←(PC)+rel	×	×	×	×	2	2
JNC rel	PC←(PC)+2, If (CY)=0, PC←(PC)+rel	×	×	×	×	2	2

JB bit,rel		PC←(PC)+3, If (bit)=1, PC←(PC)+rel	×	×	×	×	3	2
JNB bit,rel		PC←(PC)+3, If (bit)=0, PC←(PC)+rel	×	×	×	×	3	2
JBC bit, rel		PC←(PC)+3, If (bit)=1,bit←0, PC←(PC)+rel	×	×	×	×	3	2

CJNE	A, direct, rel	PC←(PC)+3,
		If (A) ≠direct, PC(PC)+rel
		If (A)<(direct), CY←1
			×	×	×	×	3	2

	A,#data,rel	PC←(PC)+3,
		If (A) ≠data, PC(PC)+rel
		If (A)<(data), CY←1
			×	×	×	×	3	2

	Rn,#data,rel	PC←(PC)+3,
		If (Rn) ≠data, PC←(PC)+rel
		If (Rn)<(data), CY←1
			×	×	×	×	3	2

	@Ri,#data,rel	PC←(PC)+3, if ((Ri)) ≠data, PC←(PC)+rel If ((Ri))<(data), CY←1	×	×	×	×	3	2
DJNZ	Rn,rel	PC←(PC)+2,Rn←(Rn)-1, If (Rn) ≠0, PC←(PC)+rel	×	×	×	×	2	2
	direct,rel	PC←(PC)+3, (direct)←(direct)-1, if (direct) ≠0, PC←(PC)+rel	×	×	×	×	3	2

Stack, empty operation class instruction

Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
PUSH direct		SP←(SP)+1, (SP)←(direct)	×	×	×	×	2	2
POP direct		direct←(SP), SP←(SP)-1	×	×	×	×	2	2
NOP		empty operation	×	×	×	×	1	1

Bit manipulation instruction

Mnemonic		Function	Impact on the flag				Number of bytes	Number of cycles
			P	OV	AC	CY		
MOV	C, bit	CY←bit	×	×	×	√	2	1
	bit, C	bit←CY	×	×	×	×	2	1
CLR	C	CY←0	×	×	×	√	1	1

	bit	bit←0	×	×	×	×	2	1
SETB	C	CY←1	×	×	×	√	1	1
	bit	bit←1	×	×	×	×	2	1
CPL	C	CY←($\overline{CY}$)	×	×	×	√	1	1
	bit	bit←($\overline{bit}$)	×	×	×	×	1	1
ANL	C, bit	C←(C)∧(bit)	×	×	×	√	2	2
	C, /bit	C←(C)∧($\overline{bit}$)	×	×	×	√	2	2
ORL	C, bit	C←(C)∨(bit)	×	×	×	√	2	2
	C, /bit	C←(C)∨($\overline{bit}$)	×	×	×	√	2	2

Pseudo-instruction		
Mnemonic	Instruction format	Function description
ORG	【tab:】ORG addr16	Define the first address of tab
EQU	tab EQU data/tab	Assign values to labels
DB	【tab:】 DB item or item tabel	Define a-byte or multi-byte
DW	【tab:】 DW item or item tabel	16 bit word content used to define two or more cells in memory
DS	【tab:】DS expression	Specifies to leave several memory cells starting with the label
BIT	tab BIT address	Assign a bit address to a label
END	END is placed at the end of the assembly language program to tell the assembler that the source program ends here.	

CPU instruction symbol table

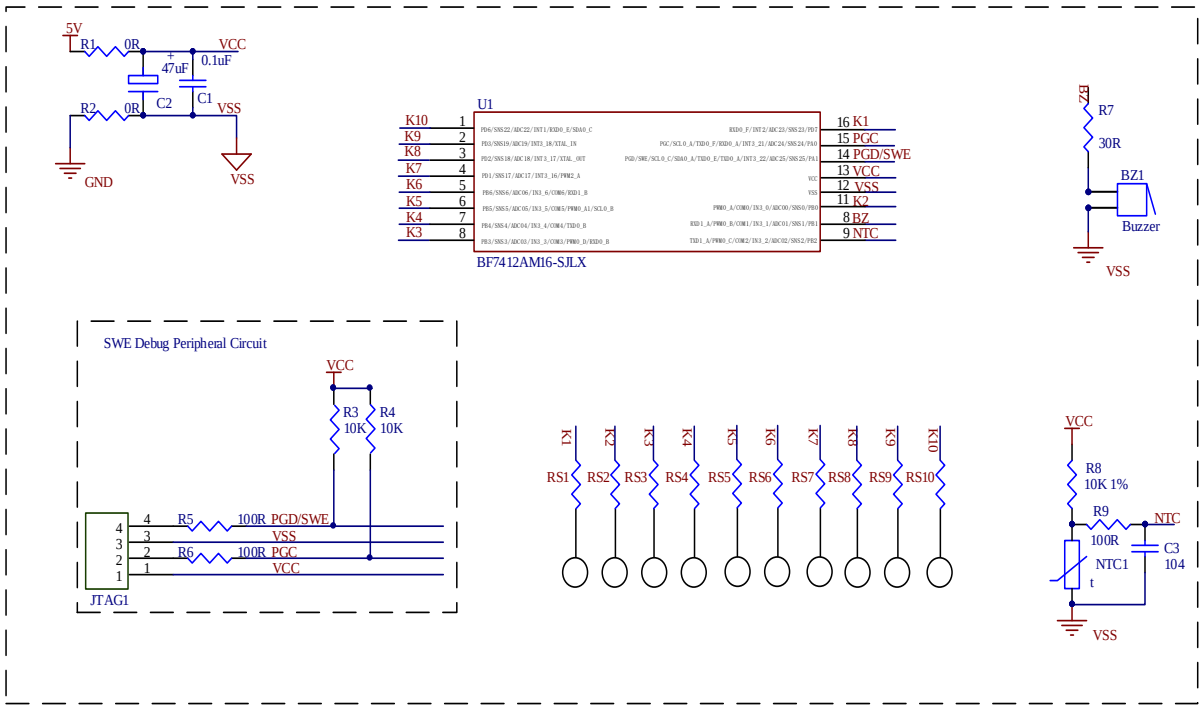
CPU related register

SFR register				
Address	**Name**	**RW**	**Reset value**	**Function description**
0x81	SP	RW	0x07	stack pointer register
0x82	DPL	RW	0x00	data pointer register 0 low 8 bit
0x83	DPH	RW	0x00	data pointer register 0 high 8 bit
0x87	PCON	RW	0x00	low power mode select register
0xE0	ACC	RW	0x00	accumulator
0xF0	B	RW	0x00	B register

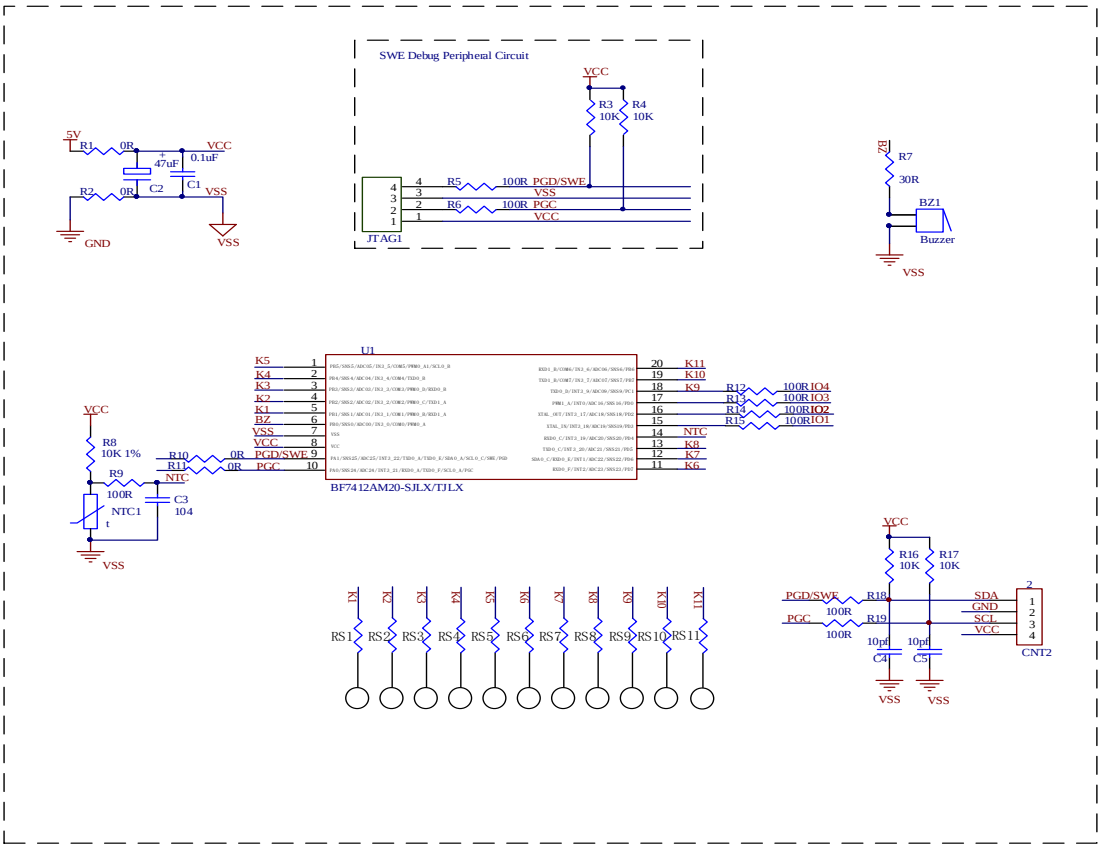
CPU SFR register list

18. Reference Application Circuits

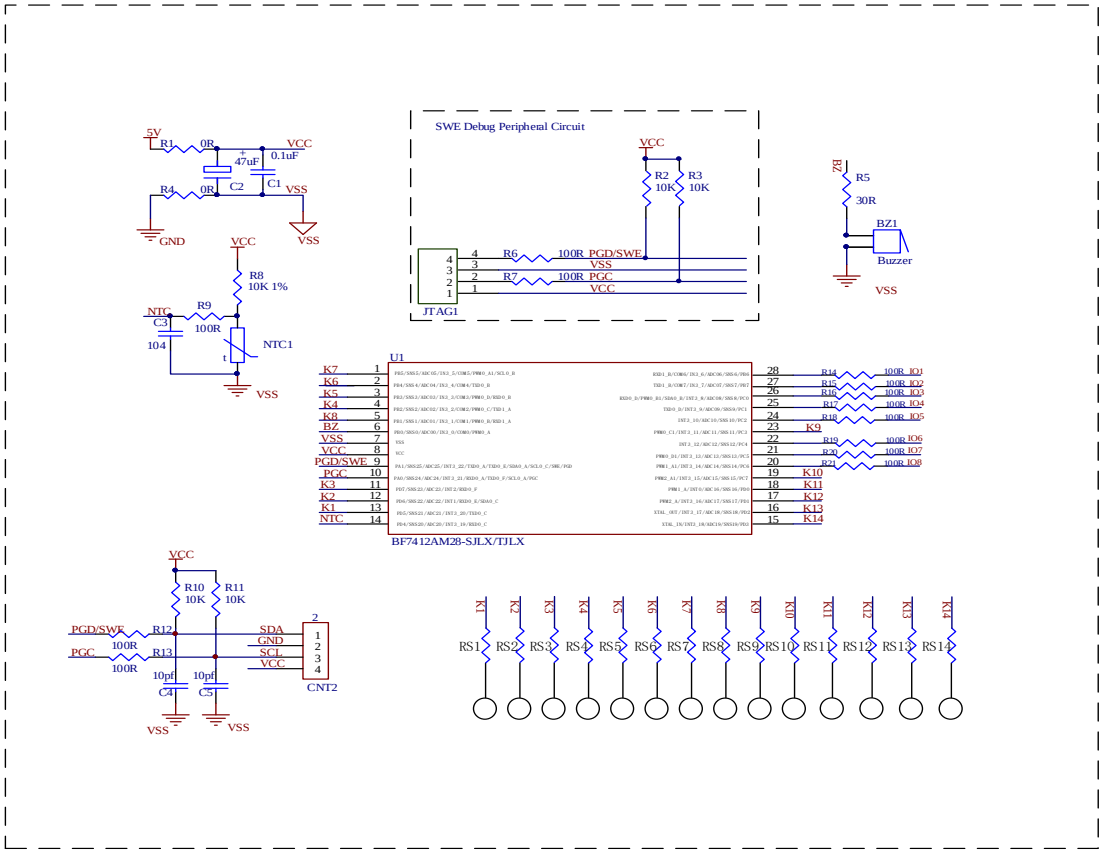
18.1. BF7412AM16-SJLX Reference Circuit



18.2. BF7412AM20-SJLX/TJLX Reference Circuit



18.3. BF7412AM28-SJLX/TJLX Reference Circuit

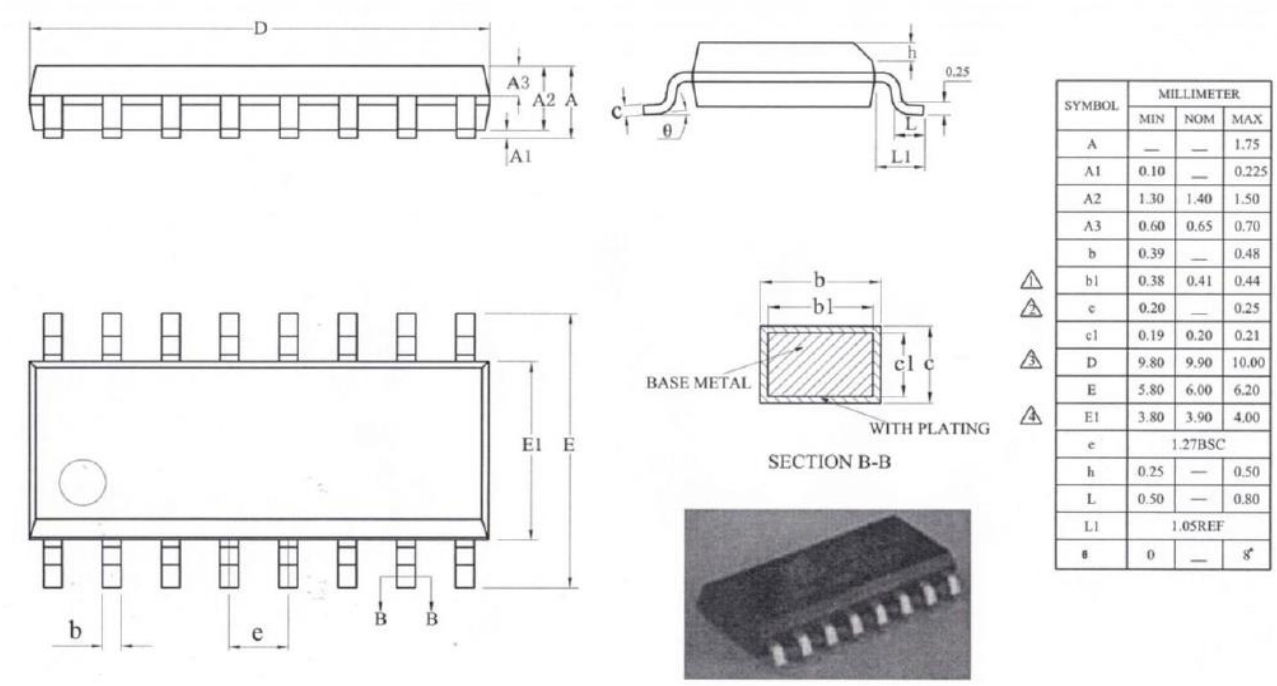


Note: The above reference schematic reference circuit is for reference design only.

1. The RSX channel resistance is recommended to be 1k~8.2k, normal 4.7k.
2. The SWE debugging peripheral circuit is only used for SWE debugging. If the emulator or adapter board has a pull-up resistor, there is no need to connect the SWE pull-up resistor.
3. Replace the 0Ω resistors with parallel power and ground with magnetic beads. The EMI test item (RE) can increase the test margin. The recommended parameter is 600 Ω@100MHz.

19. Packages

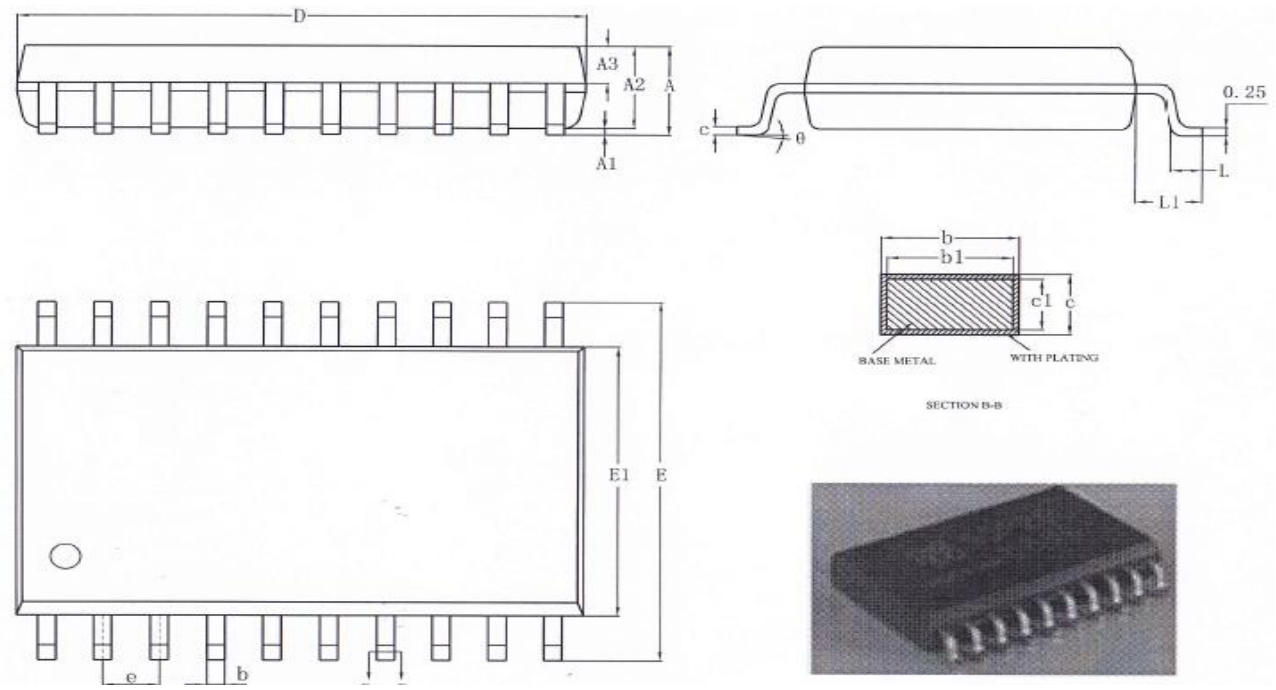
19.1. SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
⚠1 b1	0.38	0.41	0.44
⚠2 c	0.20	—	0.25
c1	0.19	0.20	0.21
⚠3 D	9.80	9.90	10.00
E	5.80	6.00	6.20
⚠4 E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

SOP16 Package Infographic

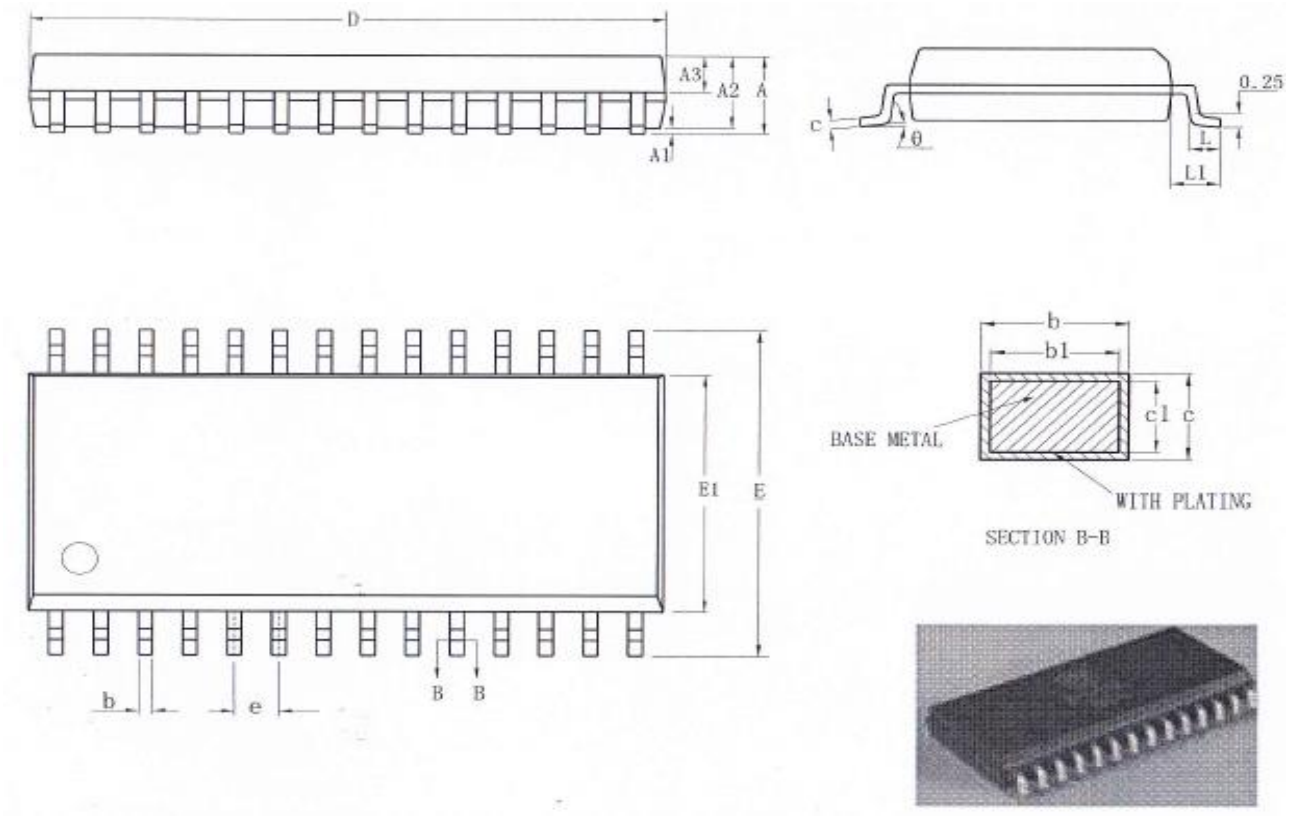
19.2. SOP20



SOP20 Package Infographic

DIM	SOP020 MILLIMETERS		
	MIN	NOM	MAX
A	-	-	2.650
A1	0.100	0.200	0.300
A2	2.250	2.300	2.350
b	0.350	-	0.440
c	0.250	-	0.310
D	12.600	12.800	13.000
E1	7.300	7.500	7.700
E	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	-	1
θ	0 °	-	8 °
End surface waste	-	-	0.2
Total length of plastic package	12.800	13.000	13.300

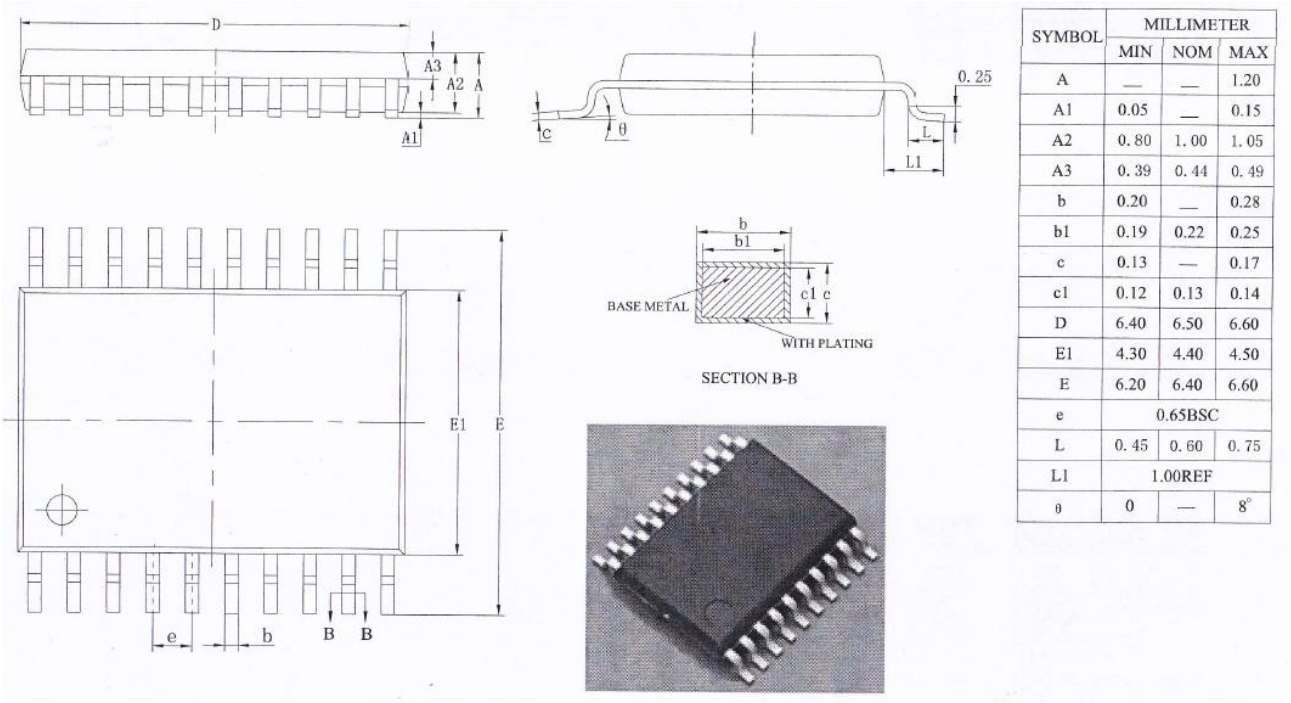
19.3. SOP28



SOP28 Package Infographic

DIM	SOP028 MILLIMETERS		
	MIN	NOM	MAX
A	2.250	2.400	2.650
A1	0.100	0.200	0.300
A2	2.250	2.300	2.350
b	0.300	0.425	0.480
c	0.250	0.285	0.310
D	17.800	18.000	18.200
E1	7.300	7.500	7.700
E	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	-	1
θ	0 °	-	8 °
End surface waste	-	-	0.2
Total length of plastic package	18.000	18.300	18.500

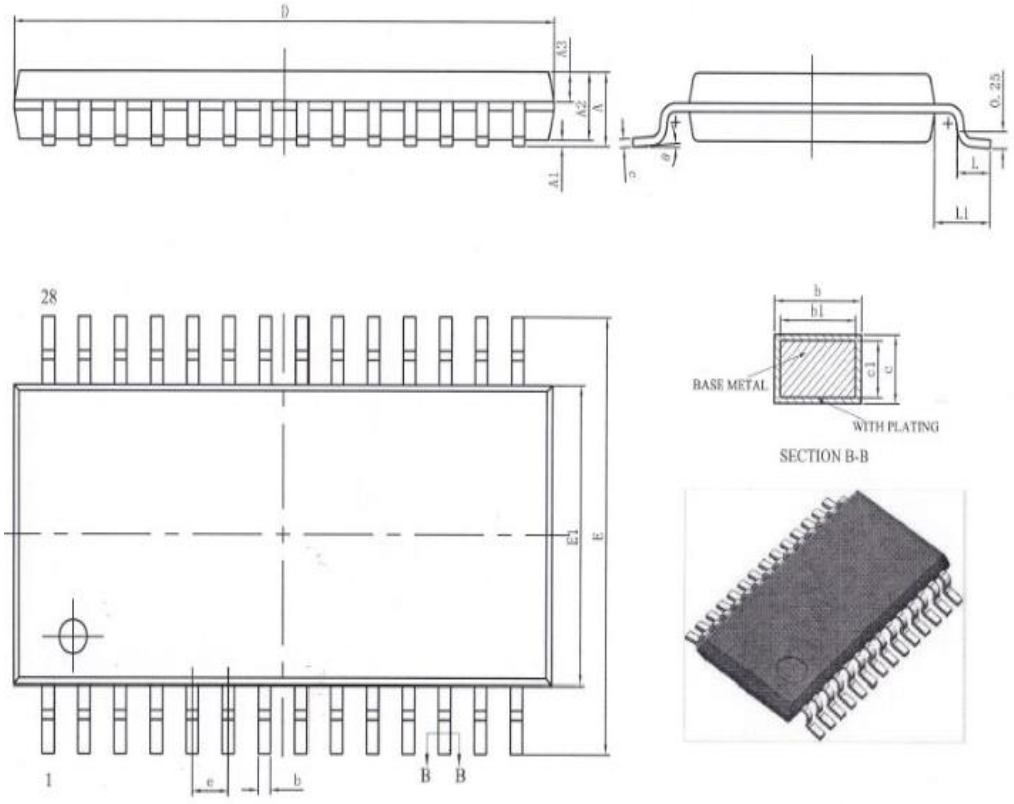
19.4. TSSOP20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	8°

TSSOP20 Package Infographic

19.5. TSSOP28



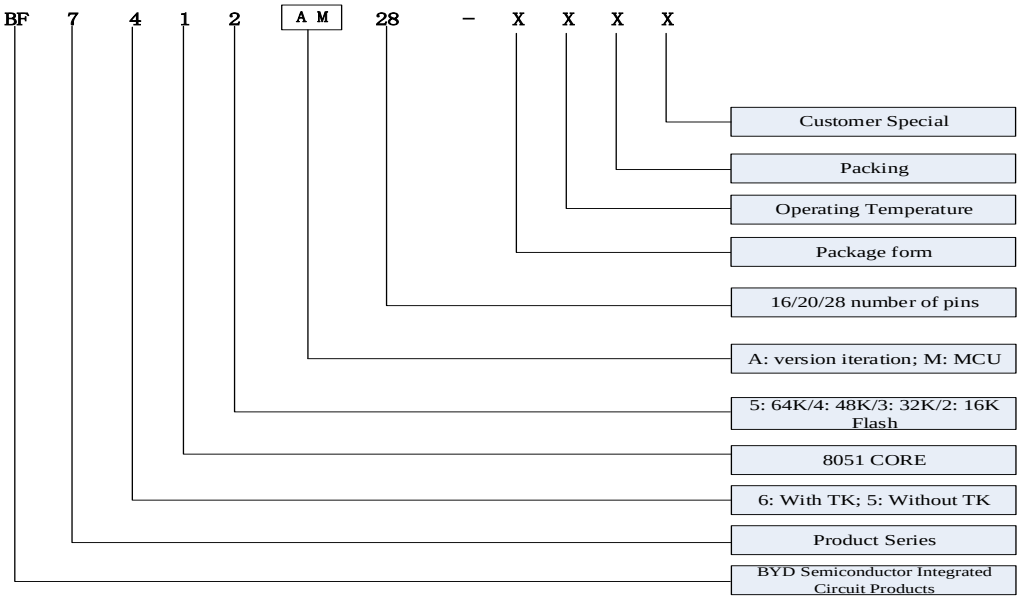
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.00
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.14	—	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

TSSOP28 Package Infographic

Ordering Information

Package	Work temperature		Package style	Keep the follow-up
S: SOP	Car grade	A: -40℃~+150℃	B: tap	-
A: SSOP		B: -40℃~+125℃	L: feed tube	-
T: TSSOP		C: -40℃~+105℃	T: tray	-
M: MSSOP		D: -40℃~+85℃	-	-
L: LQFP	Industrial grade	K: -40℃~+85℃	-	-
Q: QFN		J: -40℃~+105℃	-	-
B: BGA		L: -40℃~+125℃	-	-
D: DIP	Consumer grade	P: -25℃~+70℃	-	-
-		Q: 0℃~+70℃	-	-

Example:



Revision History

Revised date	Revised content	Reviser	Remarks
2021-06-09	V1.0	YNN	V1.0
2021-09-14	1. Add two models, BF7412AM20-TJLX and BF7412AM28-TJLX 2. Update 3.1. FLASH memory chapter 3. Update BYD LOGO 4. Update ADC conversion time formula 5. Update ADC characteristics table 6. Added section 5.3.1. Reset System Register 7. Update register 1CH, BFH, C7H, BBH, B5H, FFH description 8. Add BOR description	YNN	V1.1
2021-11-03	1. Update the power-down reset voltage range 2. Update the LVDT voltage range 3. Update register 87H, 89H, B3H, FFH description 4. Update timer 0/1 chapter	YNN	V1.2
2021-12-01	1. Update register BCH description	YNN	V1.3

Disclaimer

1. The information contained herein is subject to change without notice, see the revision record for details. Please contact FAE or the agent for the latest version.
2. BYD Semiconductor Co., Ltd. will do its utmost to ensure the high quality and high stability of the company's products. Nonetheless, due to the inherent characteristics of general semiconductor devices such as electrical sensitivity and vulnerability to external physical damage, our products may malfunction or fail under these circumstances. When using our company's products, users are responsible for designing a safe and stable system environment in compliance with safety rules. Users can avoid possible accidents, fires and public injuries by removing redundant devices, failure prevention and fire prevention measures. When the user uses the product, please follow the operating steps specified in the company's latest manual to use the product.
3. The products of BYD Semiconductor Co., Ltd. in this document are designed for general electrical applications (computers, personal tools, company tools, measuring tools, industrial mechanical devices, household appliances, etc.). The company's products can not be used in some special equipment that requires extremely high stability and quality, so as to avoid accidents such as casualties. The range of products that cannot be applied includes atomic energy control equipment, aircraft and aviation devices, transportation equipment, traffic signal equipment, combustion control equipment, medical equipment, and all safety equipment. The company shall not be responsible for any loss or injury caused by users who use it within the non-product application ranges listed above.